In the last decade, there has been a significant increase in integration density and computational complexity of processors in portable electronic systems. Increasing the portable device integration has heightened the desire to reduce device power consumption based on the time varying computational workload. Reducing power consumption has become a major challenge in the design and operation of today's portable systems. Dynamic voltage scaling (DVS) is an effective low-power design technique for reducing the power consumption of portable systems, which adjusts the supply voltage and correspondingly the clock frequency dynamically in order to obtain a minimum consumption of power to extend their lifetime use on a revolutionary scale. This paper presents an implementation of a control loop design for practical real-time DVS unit in portable systems for controlling the change in the duty cycle of the DC-DC buck converter and thereby, the voltage and frequency are regulated. MATLAB Simulation results are used to realize the controller design and verifying the range of saving power applied on realistic system workloads with varying execution times using different benchmark programs.

Keywords: Power Management, DVS Unit, PID Controller.

1. INTRODUCTION

The integrated microprocessor has been a landmark in the evolution of portable computing technology. In digital portable design, more efforts are now spent on microprocessor’s power dissipation management to maximize battery life, reduce cooling costs, and improve reliability [1].

The portable systems require functional DVS units to address high-performance computation with minimum power dissipation. Minimizing the power/energy consumption of portable systems leads to a reduction in heat dissipation and cooling requirements, which reduce design packaging and operating costs to keep the chip at an acceptable safe bound level. It has become a first-class design constraint in microprocessor's development for high-performance computing systems including advanced architectures [2].

The hardware unit of the DVS allows supply voltage as well as clock frequency to be scaled down such that the actual delay of the chip instead of worst case delay meets the target performance.

The digital loop controller design for today's portable processors is becoming highly integrated. A number of researches have been published recently in the literature, and it has gained popularity amongst researchers in recent years. Y. Zhu and F. Mueller in [3] presents a novel approach combining feedback control with DVS schemes targeting hard real-time systems with dynamic workloads, the method relies strictly on operating system support by integrating a DVS scheduler and a feedback controller within the EDF scheduling algorithm. F. Firouzi et. al. presents an accurate formula for modeling the soft error rate of a circuit under different frequency and voltage conditions in [4], the proposed formula can be exploited in reliability-aware DVS schemes for dynamic control of energy and soft error in digital circuits. G. M. Almeida et. al. in [5] proposed a novel strategy for optimizing resources in multi-processor systems-on-Chip (MPSoC), the approach is based...
on using control-loop feedback mechanism, they have demonstrated the efficiency of the proposed PID controller by presenting three different scenarios. Wentong Ye et. al. presents the design of three-layer back-propagation (BP) neural network, the algorithm of BP neural network PID controller is analyzed in [6], the results showed that the PID controller based on BP neural network has good control effect in the performance of following, anti-interference, robust. S. Zhen et. al. in [7] presents an integrated high frequency and high efficiency synchronous buck converter for DVS applications, the experimental results show that high efficiency and fast reference tracking DC-DC converter brings feasible design of DVS applications.

For ensuring low power operation, and high performance portable DVS unit guarantee, this work tries to study, design, and simulation of a digital loop for controlling the change in the duty cycle of the buck converter and thereby, the voltage and frequency are regulated, which is consistent and applicable for DVS units in allowing compact low power and fast realization of high speed portable processors.

MATLAB Simulations are used to validity of theoretical background, and fundamentals have been confirmed. Results have shown that considerable amount of power consumption reduction has been obtained.

2. PID CONTROLLER, BUCK CONVERTER, AND DVS UNIT BASICS

In high performance digital portable systems the number of transistors in a microprocessor chip has been increasing quickly and the power consumption per transistor has been increasing accordingly. The increasing of power consumption results in a raised ambient temperature. Thus the device performance is degraded and the circuit performance is less stable. Therefore, low-power/energy consumption operation has become a general trend for portable circuits and systems. In order to reduce power consumption, reduction of power supply voltage accompanied by desired clock frequency is essential and necessary [8].

Lowering both of power supply voltage and clock frequency is the most efficient method in reducing power dissipation of a CMOS processor chip, this technique is known as dynamic voltage scaling (DVS). The DVS technique offers high performance and low power approaches.

For a time varying computational workload, the DVS allows hardware to alter dynamically the voltage-frequency of the processor ($f\alpha V$). The main component of the power consumption is the dynamic power, which is proportional to ($V^2f$), and energy per cycle is power divided by frequency, energy consumption is proportional to frequency squared ($E\alpha f^2$). So, the processor for light workloads can run at half speed and thereby use (1/4) of the energy to run for the same number of cycles [9].

A variable power supply can be generated using a DC-DC buck converter which takes a fixed supply voltage and can generate a variable voltage output based on a pulse-width modulated signal (PWM) by modulating the duration of the ON/OFF pulses. The PID controller is required to improve voltage scaling algorithms so that their performance remains the same but their energy consumption goes down, hence, the buck converter will be able to achieve high efficiency at light loads. The simplified DVS unit is shown in figure 1.
Figure 1: Schematics of the simplified DVS unit

The generated frequency from voltage controlled oscillator ($f_{vco}$) is determined by the control voltage generated by the buck converter by keeping the difference between the reference voltage ($f_{ref}$) and $f_{vco}$ equal to 0. The PID controller adjusts the supply voltage $V_{dd}$ as the difference between $f_{ref}$ and $f_{vco}$, its transfer function is given by the following equation:

$$C(S) = K_p + \frac{K_i}{S} + K_d S = \frac{K_d S^2 + K_p S + K_i}{S}$$

(1)

Where, $K_p$ is proportional gain, $K_i$ is integral gain, and $K_d$ is derivative gain.

The purpose of PWM is to provide a variable DC voltage by translating the PID output in term of duty variable cycle pulses (D) that is then converted to $V_{dd}$ by the buck DC-DC converter. To regulate the battery or DC voltage into a dynamically variable voltage, high performance and power efficient PID controller is required to achieve variable frequency operation to give an improvement in efficient operating range of the DVS unit, where, conventional fixed-frequency DC-DC converters cannot meet these requirements [10].

In portable systems, DVS unit targets components that are in active state, but serving a light workload to deliver high performance systems when required. Since processor activity is variable, there are idle periods, when no useful work is being performed, and DVS eliminates these power-wasting idle times by lowering the processor’s voltage and frequency. From all these considerations, the approximate of the power dissipation on a portable CMOS circuit node gives the following formula:

$$P_{CMOS} = P_{dynamic} \approx \alpha f C V_{dd}^2$$

(2)

Where, $\alpha$ is the switching activity, and $C$ is the load capacitance [11].

The circuit delay $\Delta$, which sets the clock frequency, depends on the supply voltage:

$$\frac{1}{f} \approx \Delta \approx \frac{V_{dd}}{V_{dd} - V_t}$$

(3)

Where, $V_t$ is the threshold voltage and $\gamma$ is the saturation velocity index.

For a small $V_t$ the relation between clock frequency and supply voltage is:

$$f \approx V_{dd}^{(\gamma-1)}$$

(4)

Equation 4 indicates that, as a result, the power dissipation of digital portable devices is frequently subjecting to voltage breakdown and regulation, this condition is generally accompanied by an excessive change in clock frequency.
3. THE CONTROL LOOP: THEORY AND DESIGN

PID controller is a feedback based controller to provide the error signal and calculates the output based on the characteristics of the signal. It is widely used in the electronic circuits because of the ample use of proportional integral derivative controllers to maintain the stability of the control system. The structure of the PID controller makes it easy to regulate the process output; it can be represented in the block diagram of figure 2, and its transfer function form was given in equation 1 [5].

- The proportional term \( K_p e(t) \) drives a change to the output that is proportional to the current error for a current state of the process variable.
- The integral term \( K_i \int_0^t e(t)dt \) is proportional to both the magnitude and the duration of the error. It (when added to the proportional term) accelerates the movement of the process towards the set point and often eliminates the steady-state error that may occur with a proportional only controller.
- The derivative of the process error is calculated by determining the slope of the error over time \( K_d \frac{de(t)}{dt} \), that is multiplied by the derivative gain [12].

![Figure 2: The block diagram of PID controller](image)

Nowadays, Electronic PID control loops are used within complex electronic devices and systems for the power conditioning of a V_{dd} hopping for DVS unit, or even the power/energy monitoring and management. It is necessary to design a PID controller for adjusting the appropriated voltage/frequency of the processors at the same time, the deadline miss ratio is reduced for saving power and meeting the deadline right on time. The DVS unit will calculate an error value from the difference between the desired and obtained throughput. As output of the PID controller frequency values is indicated and send to the PWM circuit to generate variable duty cycle pulses, which will be responsible for scaling UP/DOWN the supply voltage through the use of DC-DC buck converter topology. The converter requires re-regulation of V_{dd} for a significant period of time. The switching power supply topology is shown in figure 3 [3,12].
The VCO output frequency is approximately has a linear proportion with the input voltage from the buck converter. Therefore, changing the applied voltage to the VCO results the variable frequency output. The procedure will be repeat until the obtained processor's throughput gradually gets closer to the desired throughput. Therefore, the processor actually operates on digitized samples using fixed-point arithmetic instead of operating on a fixed supply voltage. The block diagram of the controller and digital loop is shown in figure 4.

First, \( f_{\text{ref}} \) is toggled externally to evaluate the transient performance of the DVS loop. The operation of the digital control loop is depending on the difference between the two frequencies \( f_{\text{ref}} \) and \( f_{\text{vco}} \) based on the operating system workload predictor, both are feeding into counters to count number of transitions in certain period of time, results an error difference applying to the PID controller to make possible corrections to the output and converted to voltage levels via DC-DC buck converter circuit. Therefore, the regulated required voltage will operate at the desired reference clock frequency.
The DVS digital control loop has been designed completely to varying the operating supply voltages in time in conjunction with clock frequency scaling to prevent timing violations, and then, the overall loop has been simulated using MATLAB simulation program on a specific computer machine for three relative operating clock frequency (f_{clk}: 1.0, 0.75, 0.5) and corresponding relative supply voltages (V_{dd}: 1.0, 0.75, 0.5) respectively. Simulation results have confirmed that, the control loop can reduce the significant amount of power dissipation and a significant amount of power saving has been obtained.

4. SIMULATION RESULTS

The DVS control loop is able to run processors at a continual range of clock frequencies and supply voltages. The aim is to obtain a possible power dissipation reduction, for a given clock frequency there is a unique optimal supply voltage for which the circuit delay still permits the given clock frequency to operate. The range or level of available processor speeds can only be precise. Therefore, the simulation results are obtained in a continual range of speeds. The virtual clock frequency can be obtained by running different parts of a given task at different real clock frequencies.

For a given task with N operations, to determine the optimum-frequency and voltage (f_{opt}, V_{dd-opt}), first we need to determine the closest available frequencies (f_{L} and f_{H}), the task operation will run for X at f_{L} and (N-X) at f_{H}, this is shown in equations 5 and 6 respectively.

\[
\frac{f_{L}}{f_{opt}} < f_{H} \tag{5}
\]

\[
N * f_{opt} = X * f_{L} + (N - H) f_{opt} \tag{6}
\]

The task will execute all its N cycles at V_{dd1}, partly at V_{dd2}, and partly at V_{dd3}. Figure 5 shows the PWM voltage/frequency operation modes [13].

![Figure 5: The PWM voltage/frequency operation modes](image)

The Samples of the simulation results of the DVS control loop on a machine of "3.2GHz, 2.9V, 1GB SDRAM INTEL Pentium IV processor", using different benchmark programs are shown in figures 6 to 9.

Figure 6, 7, and 8 shows the 3D (V_{dd}, f_{clk}, Power) outcome plots for three different operating clock frequencies (f_{clk}: 3.2GHz, 2.4GHz, 1.6GHz) and three correspondence supply voltages (V_{dd}: 2.9V, 2.175V, 1.45V) respectively.

Figure 9 shows the 2D (V_{dd}, f_{clk}, Power) outcome plots for a fixed and variable supply voltages (V_{dd}: 2.9V, 2.175V, 1.45V) respectively.
Figure 6: The \((Vdd, fclk, Power)\) 3D plot when \(Vdd=2.9V\) & \(fclk=3.2GHz\)

Figure 7: The \((Vdd, fclk, Power)\) 3D plot when \(Vdd=2.175V\) & \(fclk=2.4GHz\)

Figure 8: The \((Vdd, fclk, Power)\) 3D plot when \(Vdd=1.45V\) & \(fclk=1.6GHz\)
Figure 6, 7, 8, and 9 shows that, the presented digital control loop for voltage scaling can provide significant and quadratic reduction on the dynamic power consumption on realistic workloads while meeting a time constraint. The simulation results showed that with variable Vdd/fclk (100%) saves 8% of the total consumed power, saves 53% of the total consumed power for variable Vdd/fclk (75%), saves 79% of the total consumed power for variable Vdd/fclk (50%) compared with the total consumed power for a fixed Vdd/fclk.

5. CONCLUSIONS

The power dissipation reduction has become an important challenge of modern computing design because of the growing use of portable computers. The DVS for scaling a supply voltage has received a lot of attention as an effective power management technique for digital portable systems.

In this paper a digital control loop has been analyzed, presented and simulated for voltage scaling applicable for real-time portable systems assuming that the core processor can vary its supply voltage dynamically, but can use only a single voltage level at a time. The results exploit the fact that, power consumption tends to drop quadratically with voltage, while the clock frequency increasing linearly satisfying the time constraint. The controller is simple to implement and allows fast transient response to step changes in speed, and stable operation over a wide range of system clock frequencies. The simulation results confirm that, the impact of DVS technique can be considered as an excellent candidate for low power and low cost designs and cannot be overlooked because of the extraordinary growth in portable electronics.

Finally, for the future evolutions of this work, the presented design methodology can be improved and further analysis can be carried on, future work in this area will focus toward a new design topology for reducing power dissipation in conjunction with thermal solutions in high performance large scale multicore/multiprocessor computers.
REFERENCES


