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A Quasi-Cyclic LDPC Based Low Complexity and Area-Efficient Communication System for IEEE 802.11n

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Abstract: - Low-density parity-check (LDPC) code, which has an excellent error-correcting performance that is close to the Shannon limit, is the most often used error correction code (ECC) for reliable and effective communication. Despite higher performance and lower decoding complexity, the main disadvantage of LDPC codes is their high encoding complexity. A significant problem is the VLSI implementation of the LDPC encoder and decoder. In this paper, structured LDPC codes—also known as quasi-cyclic low-density parity check codes—have been used since it is good bit error ratio (BER) performance and adaptable hardware execution characteristics. The Complete (Encoder-Channel-Decoder) communication system with a 1/2 code rate, 648 bits codeward length, and sub-block size of z = 27 has been constructed for the IEEE 802.11n wireless standard.

Keywords: Quasi-Cyclic,Low-density Parity Check Codes, IEEE 802.11n, Communication System.

I. INTRODUCTION

The digital communication system is used to transmit data source to destination through a wired or wireless channel, the consistency of received data depends on the channel medium. The channel medium can introduces an error in the transmitted data. Shannon proved that the reliable communication is possible only if the data rate is less than the channel capacity. Figure 1 of basic communication system showing transfer of information from source to destination. The source encoder transforms the source output to a binary digits information sequence. The role of the channel encoder is that the information sequence from the source encoder is encoded using different error detection and error correction techniques. Prior to modulation, channel encoding adds extra symbols to the data that needs to be sent. The broadcast information may be impacted by channel noise or interference, affecting certain symbols. After the received information has been demodulated, various decoding techniques are used by the channel decoder to convert the received information sequence into a binary sequence. The estimated sequence of the transmitted sequence is transformed to the destination by the source decoder.

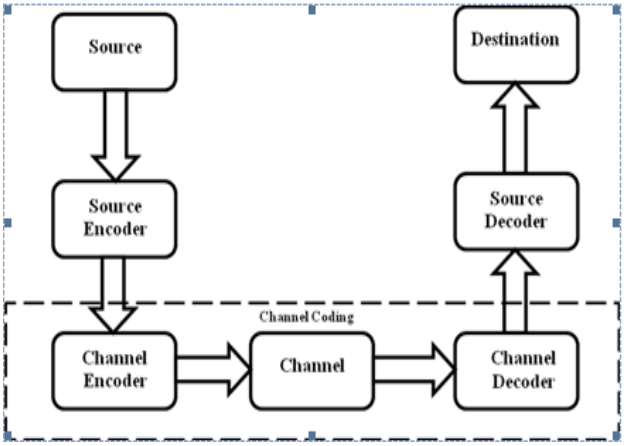

Figure.1 Basic Communication System

There are two techniques for error detection and correction: Forward Error Correction (FEC) and Automatic Repeat Request (ARQ).If there is a problem at the receiver, we must retransmit the data in ARQ. Retransmission, however,

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results in a poor throughput, expensive, and delayed system. Parity bits are extra bits of redundant information added to a message by the Forward Error Correction mechanism. The receiver can identify & fix the fault with this redundant information without sending the data again [3].

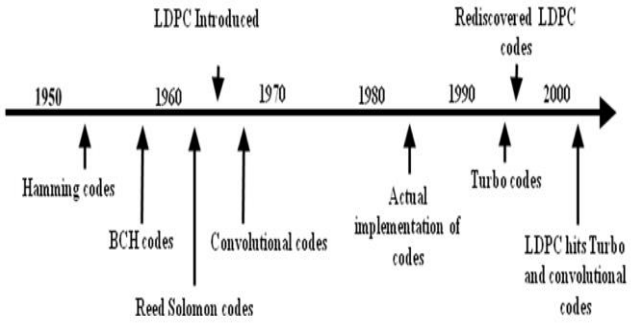

Figure2. Evaluation of error correcting codes

Forward error correction, can identify and rectify errors at the receiver end, enhancing system output, speed, and power consumption. They are appropriate for long-distance transmission, including deep space or satellite communication. Additionally, they are utilized in wireless storage and communication systems [4]. For error correction in the communication system, a variety of coding methods and error-correction algorithms may be employed. Evaluation of fault correcting codes is shown in Figure 2.

In 1950, the hamming code—the first error-correcting code—was created. Hamming codes can fix up to one-bit errors and can detect up to two-bit faults. BCH codes, a subset of cyclic error-correcting codes, were first introduced in 1959 by Hocquenghem, Bose, and Ray-Chaudhuri. The Reed-Solomon algorithm is then employed in CDs, DVDs, and hard discs due to its effective burst error correcting characteristic. Low-Density Parity Check Codes (LDPC), as they are known now, were first presented by Gallager in 1962. But up until the 1990s, it was ignored. Convolutional codes were a novel code that was introduced in between. Digital video, mobile, and satellite communications all make use of these codes. Turbo codes, which have higher error performance close to the Shannon limit, were introduced. Low-density parity-check (LDPC) codes, developed in the early 1960s by Robert Gallager, were brought back in the mid-1990s by David MacKay due to the increased decoding complexity of turbo code. With its low hardware complexity and superior error performance, LDPC codes outperform all other known codes.

Recently, there has been a lot of interest in low-density parity-check codes because of their remarkable error-correction features around Shannon's limit. These codes were mainly developed by R. Gallager in the first 1960s and revived by MacKay and Neal [2]. LDPC codes have been used in or are being considered for use in a number of present and future communication protocols, including IEEE802.11n, IEEE802.16e, DVB-S2, and IEEE802.3an. Although LDPC codes perform better and decode more easily, their biggest drawback is a challenging encoding process. An structured LDPC code can make the encoder less difficult. It is hypothesised that LDPC codes can be created by approximating an upper triangular parity check matrix, even if various encoding approaches have been employed in the past. This will greatly reduce the encoding complexity. Quasi-Cyclic Low-density Parity Check Codes, which are structured LDPC codes, are used in this work. It has been suggested that Quasi-Cyclic can be used to streamline LDPC and still produce equivalent outcomes[13].

QC-LDPC codes have a sparse parity check matrix due to the lower number of them. So, in order to streamline the encoding processes, the lower-triangular matrix approach provided by Richardson and Urbanke [3] is used. The Richardson and Urbanke encoder [2,10], which is based, offers an real linear running time for various codes with a sparse parity-check matrix[14]. The better bit error ratio (BER) performance of quasi-cyclic LDPC (QC-LDPC) structured codes over random codes has attracted a lot of attention due to its adjustable hardware implementation capabilities. In compliance with IEEE 802.11n and 802.16e standards, which permit varying communication rates and code lengths, QC-LDPC codes have been utilised recently. There are multiple decoding strategies for QC-LDPC codes in order to preserve the trade-offs between hardware complexity, decoding efficiency, and error-correction performance. The efficiency of iterative message passing techniques for error correction is excellent despite their high decoding complexity[15Despite having a relatively high decoding complexity, the best decoding performance is achieved by a Sum-Product Algorithm (SPA) based on soft judgements [5,13]. A number of changes have been suggested to make the SPA's check node function simpler. Reduced non-linear functions [6,7] and logarithmic functions [8,15] further simplify these check nodes by lowering implementation complexity. Although decoding

performance is compromised, the Min-Sum (MS) approach [7,11] further simplifies SPA's check-node procedures. In order to establish a balance between complexity and effectiveness, the MS algorithm has gone through a number of improvements [9,12], including normalised MS and offset MS decoding.

II. RELATED WORK

A high-throughput encoder architecture for Quasi Cyclic -LDPC codes for IEEE 802.11n/ac criteria was created by researchers. To achieve high throughput and minimum hardware complexity, a partially parallel encoder design is described in this study. A low complexity cyclic shifter is utilised to reduce the hardware overhead of combinational circuitry while increasing encoder throughput through the use of forward and backward accumulations. For (1944, 1620) irregular LDPC codes, the suggested encoder is developed utilising 130-nm CMOS technology. Gate count of 96K at 100 MHz clock frequency results in 7.7 Gbpsthroughput[19].

IoannisTomkos, GeorgiosTzimpragos, DimitriosSoudris, and ChristoforosKachris presented a novel design technique for QC-LDPC encoders. With this design, IEEE 802.11, IEEE 802.16, and other LDPC codes with similar properties can be developed. This paper uses a unique hardware optimisation technique based on multiplication by constant matrices in GF(2) to improve the Quasi-Cyclic LDPC encoding process. By hardwiring the signals directly into the LUTs, this method eliminates the need for the cyclic shifters and block memory that are often used. This architecture greatly speeds up encoding while utilising the fewest resources possible. The recommended encoder architecture is suitable even for high-speed applications[16].

SherifAbouZied, Ahmed TarekSayed, and RafikGuindi suggested a fully pipelined LDPC decoder for the 802.11n standard that supports different block sizes and coding speeds. By efficiently employing the permutation network for both forward and backward routing for interconnections, they streamline linkages and reduce the amount of memory bits needed. The Xilinx Virtex-6 FPGA was used to implement the decoder.This shows 12% more throughput and a 19% reduction in dynamic power and resource usage in comparison to the architecture built using the same routing technique[17].

HemeshYasotharan and Anthony Chan Carusone developed a Flexible Hardware Encoder for Systematic Low-Density Parity-Check Codes for the IEEE 802.16e WiMAX standard. They proposed a direct approach in which the generating matrix is expressed in systematic form as an alternative to the Richardson-Urbanke encoding procedure. By boosting memory use, parallelization, and faster encoding, they made computations in the architecture design simpler. At a maximum frequency of 60 MHz, the design used 11,430 logic components. From 115 Mbps to 357 Mbps, the throughput was available. The fastest flexible FPGA encoder demonstrated a throughput gain of 2.5–6 times above the state-of-the-art. [18].

To reduce the implementation complexity of decoding Low-Density Parity-Check (LDPC) codes, VikramArkalgudChandrasetty and Syed Mahfuzul Aziz presented an approach based on basic hard-decision decoding techniques. The method was validated using the IEEE 802.11n Wireless Local Area Network (WLAN) standard LDPC code simulation. By far, the recommended method can lower bit error rate (BER) more than fully hard-decision based decoding algorithms.The Xilinx Virtex 5 FPGA was used in the development and testing of the decoder, resulting in a notable decrease in hardware requirements and enabling throughput of around 16.2 Gbps with a BER performance of 10-5 at an Eb/No of 6.25 dB [20].

An IEEE 802.11n Wireless LAN Standard hybrid low-density-parity-check (LDPC) decoder is presented by MervePeyic, Hakan A. Baba, IlkerHamzaoglu, and Mehmet Keskinoz. They recommend differential shifting and submatrix reordering as two novel techniques in their work to lower the power consumption of the LDPC decoder hardware. On the LDPC decoder, they applied three distinct techniques: sub-matrix reordering, differential shifting, and glitch reduction. Utilising all three strategies together reduces the LDPC decoder hardware's overall power consumption by 23.7% and 38.98%, respectively, for block length 648 and code rate 5/6 and block length 648 with code rate 12[21].

III. COMMUNICATION SYSTEM USING QUASSICYCLIC-LDPC CODES FOR IEEE 802.11N

The block diagram of Communication System (Encoder -Channel-Decoder) using QC-LDPC codes for IEEE 802.11n is shown in Fig. 3. It consists of mainly input memory, LDPC encoder, Channel, LDPC decoder, and control unit.

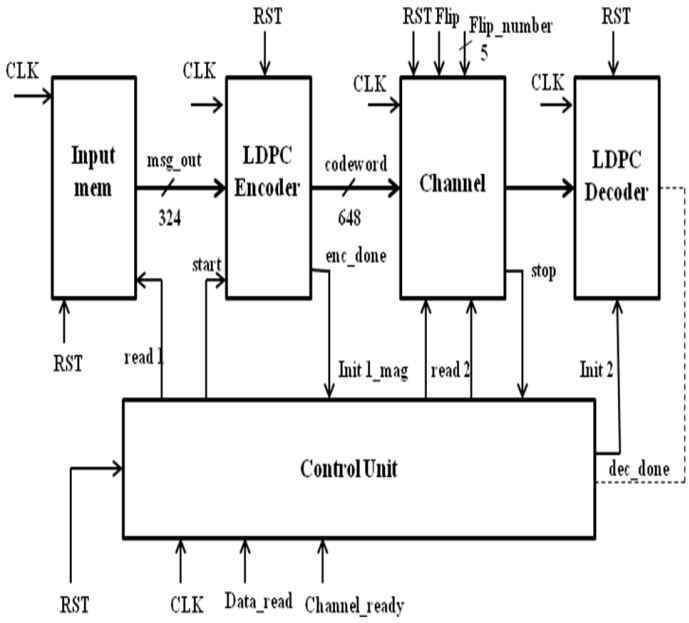

Figure.3 CommunicationSystemfor IEEE 802.11n

2.1 Input Memory

In this component input message [1:324] is stored in a register and when the control unit asserts *read* to this block the message bits are passed to the Encoder block.

2.2 Control Unit

This control unit is a Moore type FSM, the outputs are independent of the inputs and solely state dependent. There are *ten* states to this control unit which sequence trough encoding, channel modification, decoding and serial transmission of decoded message as shown in Fig.4. The ten states of this control unit in the sequence are as follows:

2.2.1 accept_msg: Whenever reset is asserted then themachine goes into this state. This makes sure that before the first active clock transition and the start of regular operation, the FSM is always initialised to a known valid state. Resets are done asynchronously. It awaits the assertion of data_read before moving on to the subsequent stage.

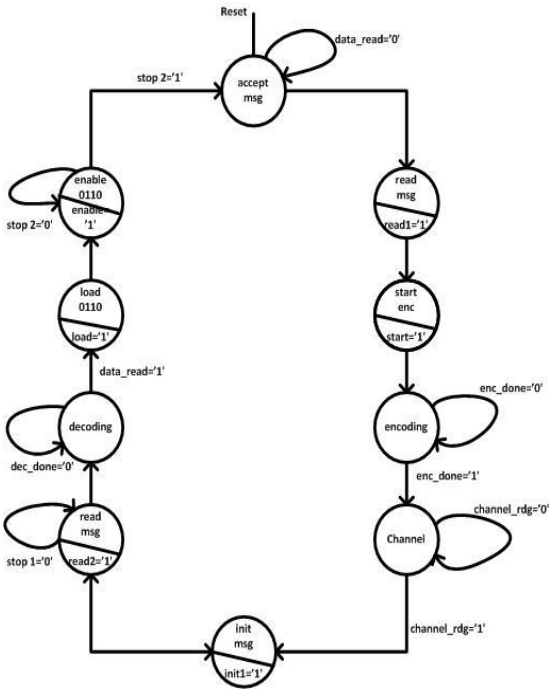

Figure 4 Finite State Machine for control unit of Communication system

2.2.2 read_msg: This state provides the read1 signal to the input memory component so that message can be passed to the Encoder. This ensures that message is waiting at the input port of Encoder and now encoding can begin.

2.2.3 start_enc: This state provides the requiredstart signal to the Encoder so that the pipelined encoding process can be initiated. This state advances unconditionally to the next state.

2.2.4 encoding: This state waits for an acknowledge signal i.e. enc_done from the Encoder component and if acknowledged then the machine transits to next state. This tells whether encoding is complete or not.

2.2.5 channel: This state is for the user to introduce a single bit error through the channel into the encoded message. It is for the user to decided if he/she wants to introduce an error or not. Whatever the case may be, this state waits for channel_rdy signal to transit to next state.

2.2.6 init_mag: This state asserts an init1 signal which initiates assigning a 4 bit magnitude to each received codeword bits. This transforms the codeword into a new frame called lambda, λ. This state advances unconditionally to the next state.

2.2.7 read_mag: This state asserts a read2 signal which starts sending the channel generated frame i.e. λ to the decoder. The decoder reads the frame and stores it in a register. When stop1 is acknowledged then it is confirmed that complete frame has been transferred to the Decoder.

2.2.8 decoding: This state waits for an acknowledge signal i.e. dec_done from the Decoder component and if acknowledged then the machine transits to next state. This tells whether correct decoding is done or not.

2.2.9. load_PISO: After successful decoding the decoded message is to be loaded into parallel in serial out shift register. This state asserts a load signal which loads the decoded message into PISO. This state advances unconditionally to the next state.

2.2.10 enable_PISO: In order to begin serial transmission of the decoded message [1:324], that is, 1, 2, 3, 4, 323, 324, an enable signal is asserted in this condition. Upon receiving this enable signal, PISO starts the serial transmission. Once stop2 is located, the decoded message's serial transmission is confirmed to have stopped. It returns to accept_msg, its starting state.

IV. RESULTS AND DISCUSSIONS

The Encoder-Channel-Decoder (ECD) system architecture was created for the IEEE 802.11n standard on Xilinx Virtex-5, Virtex-6, and Altera's Cyclone IV, DE2-115 devices. It was designed for a QC-LDPC with a block length of 648 bits and a coding rate of 12. By evaluating the routing complexity and hardware resource utilisation, the implementation challenges of the recommended LDPC decoders are judged. Fig. 5 and Fig.6 show RTL Schematic of Communication system on Virtex-5 and Cyclone IV, DE2-115 respectively.Table 1 displays an overview of the use of FPGA devices produced by the Xilinx and Altera Synthesis Tools.

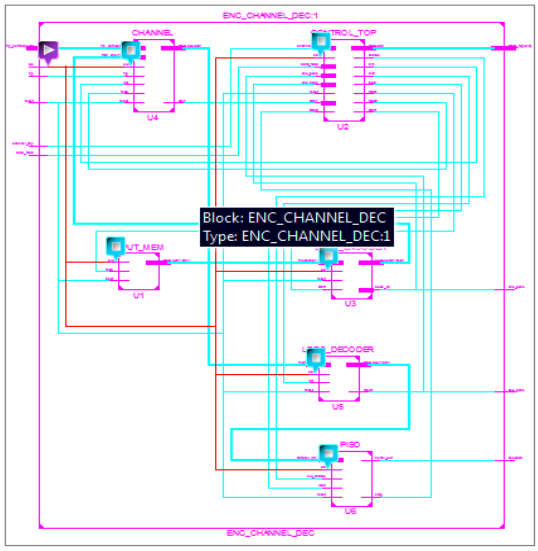

Figure 5.RTL Schematic of Communication system for IEEE 802.11n (Virtex-5)

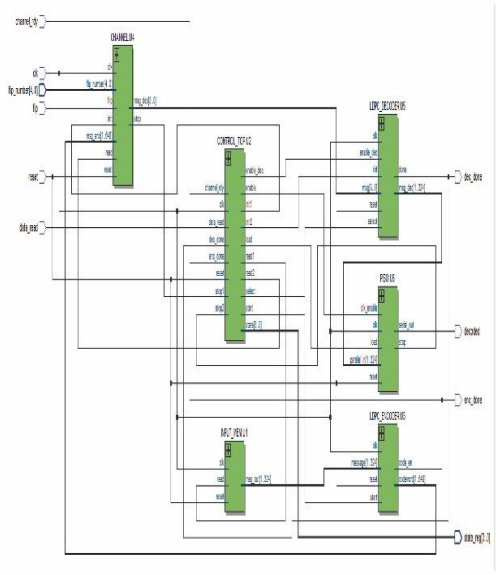

Figure 6.RTL Schematic of Communication system for IEEE 802.11n (Cyclone IV, DE2-115)

Design Summary				
		Virtex -5 XC5VLX330T FF1738-2	**Virtex-6 6VLX760FF1760-2**	**Cyclone IV, DE2-115**
Area	Number of slice registers	3388 out of 207360	4617 out of 948480	Total register 12790 out of 114480
	Number of slice LUTs	51483 out of 207360	61168 out of 474240	LE 113748 out of 117053
	Number of Fully used LUT-FF Pairs	1449 out of 53422	3009 out of 62776	Not Applicable
Max. Frequency		101.141 MHz	136.369 MHz	20.7 MHz
Power		3.476 W	4.438 W	3.695 W
Latency		64	64	64
Throughput		32Gbps	41 Gbps	25 Gbps

Table 1. Resource consumption of Communication system for IEEE 802.11n

4.1 **System Level Implementation**

The verification and testing of Encoder, Decoder on Cyclone IV, DE2-115 kit. The architectures of QC LDPC codes encoder and decoder have been implemented using Quartus II software. After the synthesis of the codes, the schematics were generated and also the blocks are verified on test benches.

4.1.1 Verification and Testing

To read out the encoded message (648 bits) in packets of 24 bits and decoded message (324 bits) in packets of 12 bits are reading out on the seven segment displays hexadecimal value will be displayed. Only six digits are used to display maximum 27 packets which are 24 bit wide are shown in Table 2 .

Address (Location)		Hexadecimal Value (24 bits: 6 digits)
0	00000	d9da7b
1	00001	ea1a31
2	00010	d8abe2
3	00011	a27b4e
4	00100	855c5c
5	00101	5c50ed
6	00110	00c483
7	00111	88ea9b
8	01000	0fb7c2
9	01001	04c2c1
10	01010	2d3997
11	01011	157a6f
12	01100	c8e4bb
13	01101	e43dbf
14	01110	9ada21
15	01111	b31d1d
16	10000	cc3e52
17	10001	120b3f
18	10010	aac201
19	10011	de829a
20	10100	29424a
21	10101	871d86
22	10110	7e168b
23	10111	646768
24	11000	ffe45c
25	11001	db0c62
26	11010	1a23c6

Table 2.Values Verified on Altera's Cyclone IV DE2-115 board

Some verified values on Altera's Cyclone IV DE2-115 board as shown in Figure 7 to Figure 11 .

Figure 7: Initial state

Figure 8 Output for 00001 address

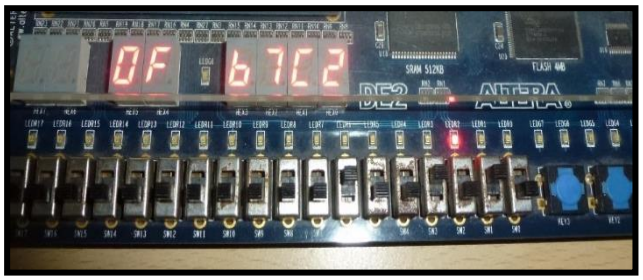

Figure 9 Output for 01000 address

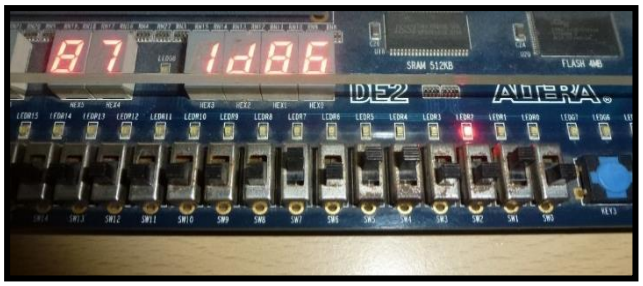

Figure 10 Output for 10101 address

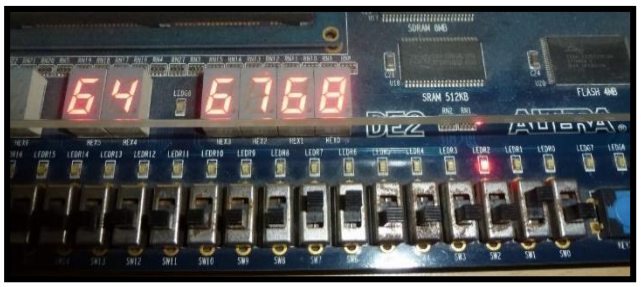

Figure 11 Output for 10111 address

V. CONCLUSION

Quasi-cyclic LDPC codes that are very close to Shannon's limit provide the best performance. Different approaches to LDPC encoding and decoding were investigated in order to create high-performing hardware. Quasi Cyclic-LDPC codes for the IEEE 802.11n standard with a 1/2 coding rate, a 648 bits codeword length, and a sub-block size of z = 27 have been selected in order to establish a communication system. On a Xilinx ISE platform, the encoder-channel-decoder for Quasi Cyclic -LDPC codes was implemented. Several details have been documented, such as throughput and resource utilisation. The Quasi Cyclic-LDPC encoder and decoder for IEEE 802.11n has been tested using Altera's Cyclone IV, DE2-115 board. The outcome demonstrates that the system architecture has less area-specific complexity. With a reasonable throughput, the encoder channel decoder design as a whole also uses fewer resources.

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