

¹Dhaval N. Patel
²Dharmesh J. Shah

A Novel Dung Beetle Optimization Approach for Automatic CMOS Analog Circuit Design



Abstract: - The main objective of the automated circuit sizing technique is to deal with the challenges of design tradeoffs in analog circuit design with improved accuracy and efficacy. Analog circuit design represents a multi-objective optimization challenge, where designers must properly balance various performance factors such as input and output impedance, power dissipation, area, unity-gain bandwidth, slew rate, and open-loop DC gain. Traditional design equations provide a sizing of differential amplifier MOS transistors, further optimization can be achieved through the application of meta-heuristic search techniques. Meta-heuristic search techniques can be used as local optimizers in a smaller search area to improve the optimization of design parameters. The differential amplifier circuit with current mirror load is optimized through the application of the Dung Beetle Optimization (DBO) algorithm. By using an evolutionary algorithm called DBO, all the required parameters were achieved with the least amount of transistor area and power dissipation when compared to the results of the Seeker Optimization Algorithm (SOA), Opposition based Harmony Search Algorithm (OHS), craziness-based particle swarm optimization (CRPSO), and Cuckoo Search (CS) algorithms.

Keywords: Complementary metal oxide semiconductor, Dung Beetle optimization, Seeker Optimization, Particle swarm optimization, Opposition based Harmony Search, Cuckoo Search, Differential amplifier with current mirror load

I. INTRODUCTION

The fundamental component of any electronic device that we might use daily, including appliances, industrial automation, communications, automotive, and computing devices, is the analog circuit. Designing any CMOS based analog circuit is a complex design process therefore an extremely essential and decisive task performed by the engineers. Several attempts have been made to improve the structure of analog circuit design [1] The difficult task of combining digital and analog circuitry on a single chip has become harder as the scale size of CMOS technology has decreased. Even though there are fewer analog circuit components in integrated circuits than in digital circuits, the design process for analog circuits in ICs is more difficult and complex. Because of the limitations imposed by the scaling of CMOS technology, creating analog circuitry has become more difficult and time-consuming, requiring specialized knowledge [2]. Several researchers and technologists have tried numerous times to optimize the architecture of analog circuits. To construct an analog circuit, one typically follows these stages, selecting a topology, optimization using parametric data, and creation of layouts. For the successful design of the analog circuit, it is advisable to follow three phases to attain the required parameters and physical arrangement at the schematic level [3].

Developing sophisticated analog circuits with ultimate performance requires a deep understanding of transistor scaling. The CMOS based automatic analog circuit design method needs stable and consistent optimization strategies achieved by adjusting the aspect ratio of transistor width and length [4], [5]. Circuit design automation systems can be classified into two categories based on their approach to circuit scaling: one category knowledge-based employs a predefined set of rules, while the other employs optimization algorithms to ascertain the most efficient design. In knowledge-based techniques depending upon circuit topology, circuit developer applied design equations based on their understanding of analog circuit design rules. Since a large amount of human work is needed for producing analytical equations and heuristics, the outcomes are often erroneous and poor. As computer power expanded, a different method known as optimization-based synthesis emerged. This method uses search methods to turn the issue into a function optimization problem. The solution is meant and generate specific results.[6], [7].

Optimization techniques are often divided into two categories: deterministic and meta-heuristic techniques. Deterministic optimization techniques were created over several decades for a variety of real-world applications. Analog circuit optimization successfully employs a few well-known mathematical techniques. This strategy has

¹ * Department of Electronics and Communication, L.D. College of Engineering, Ahmedabad, Gujarat, India. Email: dnpatel@ldce.ac.in

² Provost, Indrashil University, Mehsana, Gujarat, India.

several drawbacks, including a good starting point, stagnation in the local minimum search area, and reliance on the ongoing targeted function. Swarm intelligence algorithms, also known as population-based metaheuristics optimization algorithms, constitute the second strategy [8], [9].

Their robust, nature-inspired behavior, ease of execution, and great versatility in achieving the best results have drawn a lot of attention to the development of analog circuit design. Novel dung beetle optimization metaheuristic algorithms are investigated for developing differential amplifier circuits with outstanding performance in this article.

II. DUNG BEETLE OPTIMIZER

The outstanding coordination that dung beetles display in their colonies is used as a framework for the DBO algorithm. Designed with several position updating rules ball-rolling, dancing, foraging, thieving, and breeding activities of dung beetles are intended to provide high quality outcomes. The DBO population categorization and boundary selection techniques allow the algorithm to take into account both local convergence and global exploration.

A. Rolling Dung Beetles

It is a well-known fact that dung beetles can mold dung into spherical balls and then roll them to a suitable location. The dung beetle uses celestial cues, such as the direction of the wind or the position of the sun, to move in an accurate, straight route while steering the dung ball. The position modification equation for rolling dung beetles is as follows:

$$xi(t + 1) = xi(t) + \alpha \times k \times xi(t - 1) + b \times \Delta x \quad (1)$$

$$\Delta x = |xi(t) - X_{worst}| \quad (2)$$

where $xi(t)$ indicates the position details of the i th beetle during the t th iteration. α denotes a natural coefficient has a value of either -1 or 1, k represents the deviation coefficient in the range (0,0.2), b represents a constant in the interval (0,1), Δx is employed to imitate variations of light intensity, and X_{worst} denotes the global worst position.

B. Dancing Dung Beetles

A dung beetle will dance to adjust its direction of walking when it comes across an obstacle that forbids it from moving ahead toward a new path. For a new rolling direction, the tangent function is utilized to recreate the dung beetle's dancing tendency. Thus, the Dancing Dung Beetle's position changes as follows:

$$xi(t + 1) = xi(t) + \tan(\theta) | xi(t) - xi(t - 1) | \quad (3)$$

Where the angle represented by θ varies from 0 to π . The position of the dancing dung beetle will not be changed if θ is either 0 or $\pi/2$.

C. Breeding dung beetles

For the process of laying their eggs, female dung beetles gently move their dung balls to a safe area. This ensures that their young will develop without any danger. She lays eggs in suitable areas to have more babies. A technique for choosing borders that mimics the places where female dung beetles lay their eggs is proposed based on the spawning tactics. The following formula can be used to change your position.

$$x_i(t + 1) = X^* + b_1 \times (x_i(t) - Lb^*) + b_2 \times (x_i(t) - Ub^*) \quad (4)$$

$$Lb^* = \max(X^* \times (1 - R), Lb), \quad (5)$$

$$Ub^* = \min(X^* \times (1 + R), Ub)$$

where X^* denotes the current local optimal position, $R = 1 - t/T_{max}$, T_{max} represents the maximum number of iterations, Lb^* and Ub^* represents the lower and upper bounds of the spawning area of the optimization problem respectively.

D. Small dung beetles

A few adult dung beetles emerge from the ground in looking for feeding. We called them small dung beetles. we need to define the ideal foraging region to direct the small beetles. The following defines the perimeter of the ideal foraging area:

$$Lb^b = \max(X^b \times (1 - R), Lb) \quad (6)$$

$$Ub^b = \min(X^b \times (1 + R), Ub)$$

$$x_i(t + 1) = x_i(t) + C_1 \times (x_i(t) - Lb^b) + C_2 \times (x_i(t) - Ub^b) \quad (7)$$

The following parameters and objectives are taken into account when designing a differential amplifier:

- Design of $\frac{W1}{L1} = \frac{W2}{L2}$ width-to-length ratio to meet Av requirements
- Design of $\frac{W3}{L3} = \frac{W4}{L4}$ width-to-length to achieve the upper ICMR
- Design of $\frac{W5}{L5} = \frac{W6}{L6}$ design to width-to-length to achieve the lower ICMR
- Finding out $Id5$ (I_{ss}) range to satisfying both SR and $Pdiss$.

IV. TEST SETUP FOR AUTOMATIC ANALOGUE CIRCUIT DESIGN

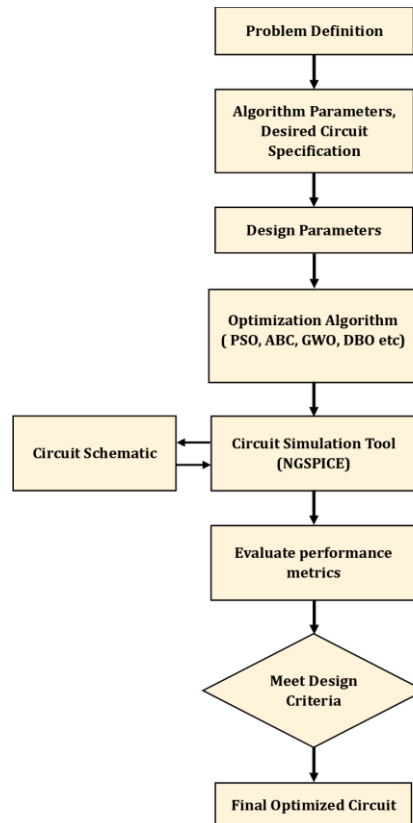


Fig 2. Flow chart for designing automatic circuits

This work aims to decrease the total CMOS transistor area under the restrictions of design variables and design requirements using the DBO algorithm. Figure 1 illustrates the automated CMOS analog circuit design test setup. The optimizer designs CMOS-based analog circuits for required specifications using an algorithm and a circuit simulator. The circuit's desired performance parameters are determined. These serve as a target for the optimization process. Through the systematic variation of individual parameters within their pre-defined limitations (upper and lower bounds), the optimization approach finds circuit designs. When creating CMOS analog circuits, the channel length (L) and channel width (W) of every PMOS and NMOS transistor are crucial parameters to consider because they have a substantial impact on circuit efficiency. The fitness function is defined as follows and is calculated by examining the simulation data from the circuit simulator.

$$F_{\epsilon} = \sqrt{\sum \left(\frac{Spec\ Desired - Spec\ Sim}{Spec\ Desired} \right)^2} \quad (9)$$

A fitness function is used to evaluate the circuit's performance [21]. The process ends if this value satisfies the termination requirements. Common criteria include minimizing the fitness function value to a sufficient degree or attaining a maximum number of iterations. If the specified termination requirements are not satisfied, the optimization process will produce an updated set of design parameters that fall within their allowable ranges [22]. To satisfy the termination requirements, the process iterates, developing designs and evaluating them. The algorithm runs until the error value is above 1e-5 or the iteration number is 100. To optimize the DA circuit, in this study, the

performance of the dung beetle optimization (DBO) algorithm is evaluated. A distinct method will be developed to optimize the differential amplifier (DA) design based on predefined criteria. The aim is to examine the degree to which they meet the standards of performance that are required.

V. SIMULATION RESULTS AND DISCUSSIONS

Python is utilized in this research to investigate how well a CMOS circuit of differential amplifier with current mirror load designed optimally and performs on an Ubuntu computer with an Intel Core i5-8265U processor operating at a frequency of 1.60 GHz and RAM size is 8 GB. To find the optimal solution of DA circuit for both the 0.18 μm and 0.35μm CMOS technologies with predefined design specifications simulations were carried out using NGSPICE software. This study's three main objectives were to decrease power dissipation, optimize amplifier gains, and minimize MOS transistor area overall while keeping the relevant design requirements and standards. The MOS transistors have been sized carefully to lessen the effect of channel length modulation. L5 and L6 employ shorter lengths of 1.4mm, while transistors L1, L2, L3, and L4 use longer lengths of 3.5mm[19]. This circuit is designed for 0.18μm CMOS technology with a power supply of ±1.8 volts and 0.5 pF capacitance, and for 0.35μm CMOS technology with a power supply of ±2.5 volts and 0.5 pF capacitance. The CMOS differential amplifier with current mirror load circuit required specifications are Av, UGB, PM, positive PSSR, negative PSSR, RSR, FSR, CMRR, P_{diss}, and total MOS transistor area (TTA). Minimizing size and power dissipation in analog circuits are both critical for building efficient and compact electronic systems. In this study, our main objective is to minimize these quantities using the DBO algorithm.

Table 1. Optimal design parameters for 0.35 μm technology CMOS differential amplifier circuit with current mirror load

Sr. No.	Set of design variables	Range of design parameters	Achieved values				
			PSO [18]	SOA [23]	OHS [24]	CRPSO [25]	DBO
1	$W_1/L_1 = W_2/L_2$ (μm/ μm)	(W) 3.5 to 30	29.4/3.5	24.5/3.5	27.99/3.5	38.5/3.5	30.00/3.5
2	$W_3/L_3 = W_4/L_4$ (μm/ μm)	(W) 3.5 to 30	11.3/3.5	7.5/3.5	10.5/3.5	12.3/3.5	3.50/3.5
3	W_5/L_5 (μm/ μm)	(W) 3.5 to 30	4.2/1.4	3.4/1.4	4.3/1.4	3.9/1.4	10.20/1.4
4	W_6/L_6 (μm/ μm)	(W) 3.5 to 30	4.2/1.4	4.8/1.4	4.8/1.4	5.8/1.4	10.20/1.4
5	I_{bias} (μA)	3.5 μA to 30 μA	125	116.8	118.31	125	8.70

Applying the suggested DBO method, a differential amplifier with specific design parameters is designed. According to the simulation results, the design parameters effectively satisfy the given design criteria. Table 1 provides the results achieved for the DA circuit employing 0.35 μm CMOS technology with various evolutionary algorithms (EAs) utilized in this study. The best design parameters of differential amplifier from the many EAs were used for validation. Table 2 lists the specifications derived using the Ngspace simulator for the obtained design parameters. Table 2 indicates an improvement over earlier research in the DBO-based design of the differential amplifier circuit.

Table 2. Simulation results and desired criteria for DA in 0.35 μm CMOS technology using various EAs

Sr. No.	Specifications	Expected value	Obtained Specifications				
			PSO [18]	SOA [23]	OHS [24]	CRPSO [25]	DBO
1	A_v (dB)	>40	42	44.02	43.45	44.49	45.33
2	UGB (MHz)	>10	10	10.48	10.63	10.03	25.34
3	PM (°)	>45	83.80	83.73	83.44	81.71	57.86
4	+ve PSSR (dB)	>40	40.10	60.79	46.19	46.43	45.87
5	-ve PSSR (dB)	>70	68.00	108.6	93.5	91.29	80.59
6	RSR (V/μs)	>10	22.4	12.28	14.37	14.19	15.00
7	FSR (V/μs)	>10	-	-	-	-	11.50
8	CMRR (dB)	>70	84.2	83.17	86.64	84.44	75.15
9	P_{diss} (μW)	<1,000	1260	559.5	668.7	580.6	35.03
10	TTA (μm ²)	<400	296	235.48	282.17	369.18	263.06

Our cost function aims to reduce the overall component area to below $300 \mu\text{m}^2$ and minimize power dissipation while ensuring all requirements are met. The differential amplifier attains a 45.33 dB gain and a 25.34 MHz UGB. The results presented are compared with the most recent studies, PSO [18], Seeker Optimization Algorithm (SOA) [23], Opposition based Harmony Search Algorithm (OHS) [24], craziness-based particle swarm optimization (CRPSO) [25]. From the comparison, it's obvious that DBO beats other algorithms in optimizing analog circuits, obtaining a transistor area of $263.06 \mu\text{m}^2$. The power consumption of $35.03 \mu\text{W}$ is achieved by this method, and its dissipation is about 94% less than that of the best-performing methods from previous studies.

Table 3. Optimal design parameters for 0.18 μm technology CMOS differential amplifier circuit with current mirror load

Sr. No.	Set of design variables	Range of design parameters	Achieved values			
			DE [26]	PSO [27]	CSPSO[28]	DBO
1	$W_1 = W_2(\mu\text{m})$	3.5 to 30	8.78	27.34	21.26	25.73
2	$W_3 = W_4(\mu\text{m})$	3.5 to 30	63.47	9.24	4.57	3.5
3	$W_5 = W_6(\mu\text{m})$	3.5 to 30	54.16	29.07	10.08	8.54
4	$I_{bias}(\mu\text{A})$	$1 \mu\text{A}$ to $200 \mu\text{A}$	22.43	10	5.52	8.12

Table 4. Simulation results and desired criteria for DA in 0.18 μm CMOS technology using various EAs

Sr. No.	Specifications	Expected value	Obtained Specifications			
			DE [26]	PSO [27]	CSPSO [28]	DBO
1	$A_v(\text{dB})$	>40	25.66	40.23	40.59	41.01
2	UGB (MHz)	>10	-	24.58	25.23	22.65
3	PM ($^\circ$)	>45	90.36	47.03	47.68	49.95
4	+ve PSSR (dB)	>40	-	40.98	41.31	41.28
5	-ve PSSR (dB)	>70	-	69.97	70.11	69.49
6	RSR (V/ μs)	>10	26.08	26.31	21.94	14.32
7	FSR (V/ μs)	>10	14.61	18.25	17.16	10.00
8	CMRR (dB)	>70	44.64	69.32	70.06	69.55
9	$P_{diss}(\mu\text{W})$	$<1,000$	-	53.74	44.34	39.77
10	TTA (μm^2)	<400	54.34	337.40	248.95	228.52

The outcomes obtained for the DA circuit using 0.18 μm CMOS technology with the different evolutionary algorithms (EAs) used in this investigation are shown in Table 3. The obtained specifications of the differential amplifier are shown in Table 4. When compared to the results obtained by the DE, PSO, and CSPSO algorithms, the DBO method achieved all specified parameters with the lowest total transistor area (TTA) of $228.52 \mu\text{m}^2$ and the lowest power dissipation (P_{diss}) $39.77 \mu\text{W}$. Important characteristics like gain, power dissipation, and transistor area are successfully optimized using this method. Compared to the optimal design parameters found in previous articles, it achieves the maximum gain of 41.01dB while lowering power consumption by around 10% and needing the least amount of transistor area. Overall, the DBO approach appears to be a useful tool for creating tiny, high-performance differential amplifiers that consume little power for 0.18 μm and 0.35 μm CMOS technology.

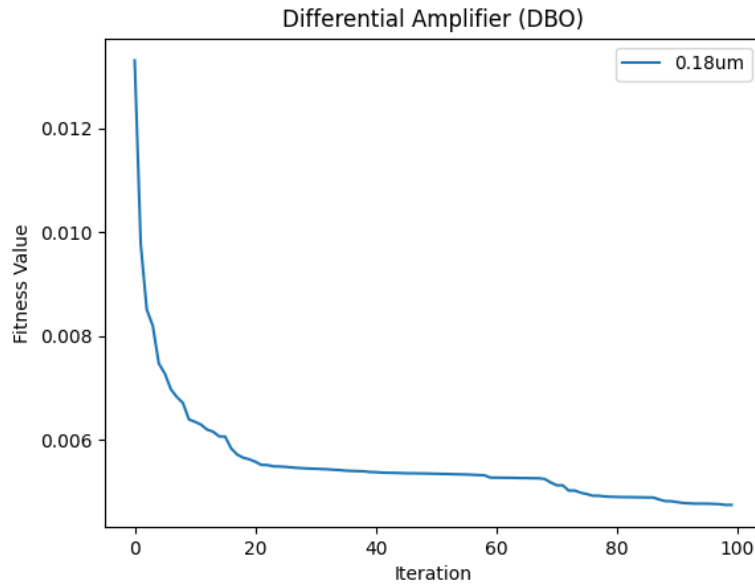


Fig 3. Convergence curve for DBO algorithm for DA circuit employing 0.18 μm CMOS technology

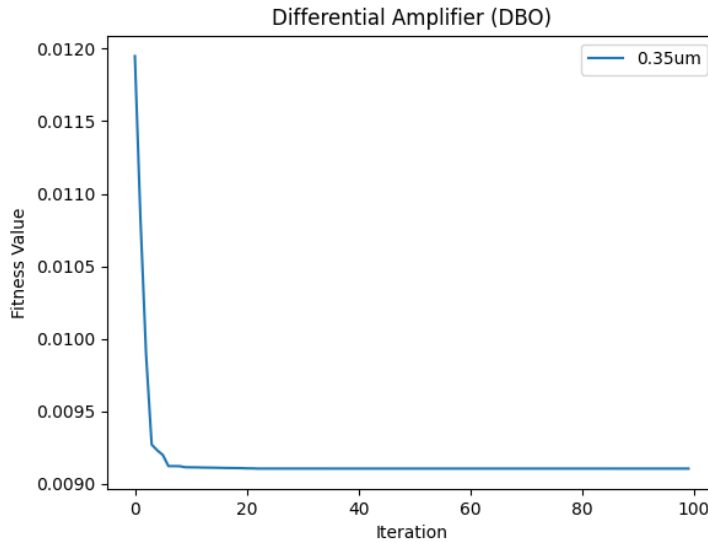


Fig. 1 Convergence curve for DBO algorithm for DA circuit employing 0.35 μm CMOS technology

The convergence rates of differential amplifier circuits created utilizing the two distinct CMOS technologies of 0.18 μm and 0.35 μm are probably compared in Figs. 3 and 4. Differential amplifier circuits can be effectively optimized with the help of the DBO method. To maximize circuit performance, it focuses its efforts during the first 20% of the iteration process.

Table 5. Computational performance of DBO algorithm

Parameters	CMOS Technology	No. of swarms	No. of Iteration	Fmin	Fmax	Fmean	Fstd
Values	0.35 μm	30	100	4.86E-03	5.77E-03	5.05E-03	3.23E-04
	0.18 μm	30	100	3.28E-03	1.08E-02	4.75E-03	2.61E-03

Table 5 provides the computational performance of DBO algorithm for DA circuit employing 0.18 μm and 0.35 μm CMOS technologies. Figure 3 and Figure 4 show the convergence performance of the DBO algorithms of a differential amplifier.

VI. CONCLUSION

Analog CMOS circuit automation is a challenging and time-consuming task, tackled by employing an evolutionary optimization technique based on the DBO algorithm to optimize circuits, such as a CMOS differential amplifier. Furthermore, integration of the DBO algorithm into our Ngspice tool enables optimal sizing of analog circuits through simulation-based optimization in Python. Aiming to achieve all targeted specifications such as higher voltage gain, better frequency response, smaller area, and lower power consumption. The DBO-based design approach is implemented to develop differential amplifier designs with current mirror loads for TSMC 0.35 μ m and 0.18 μ m CMOS technologies. These designs not only satisfy all design requirements, but they also use less transistor space and power dissipation overall than the previous approaches.

REFERENCES

- [1] A. Abraham, 2009 World Congress on Nature & Biologically Inspired Computing : 9-11 December 2009, Coimbatore, India : proceedings. IEEE, 2009.
- [2] Kubař, M. & Jakovenko, Jiri. A Powerful Optimization Tool for Analog Integrated Circuits Design. *Radioengineering*. 22. 921-931,2013.
- [3] Jafari, A., Sadri, S., & Zekri, M. (2010). Design optimization of analog integrated circuits by using artificial neural networks. 2010 International Conference of Soft Computing and Pattern Recognition, 385–388. <https://doi.org/10.1109/SOCPAR.2010.5686736>
- [4] P. Kumar and K. Duraiswamy, “An Optimized Device Sizing of Analog Circuits using Particle Swarm Optimization,” *Journal of Computer Science*, vol. 8, no. 6, pp. 930–935, 2012.
- [5] P. K. Meduri and S. K. Dhali, “A methodology for automatic transistor-level sizing of CMOS OpAmps,” in *Proceedings of the IEEE International Conference on VLSI Design*, 2011, pp. 100–105. doi: 10.1109/VLSID.2011.53.
- [6] Ö. S. Sönmez and G. Dündar, “Simulation-based analog and RF circuit synthesis using a modified evolutionary strategies algorithm,” *Integration, the VLSI Journal*, vol. 44, no. 2, pp. 144–154, Mar. 2011, doi: 10.1016/j.vlsi.2010.11.001.
- [7] E. Afacan, S. Ay, F. V. Fernandez, G. Dündar, and F. Basckaya, “Model based hierarchical optimization strategies for analog design automation,” *EDAA*, Apr. 2014, pp. 1–4. doi: 10.7873/date.2014.027.
- [8] A. Zemliak, “Analog circuit optimization on basis of control theory approach,” *COMPEL - The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, vol. 33, no. 6, pp. 2180–2204, 2014, doi: 10.1108/COMPEL-10-2013-0324.
- [9] M. Dehbashian and M. Maymandi-Nejad, “A new hybrid algorithm for analog ICs optimization based on the shrinking circles technique,” *Integration, the VLSI Journal*, vol. 56, pp. 148–166, Jan. 2017, doi: 10.1016/j.vlsi.2016.09.009.
- [10] J. Xue and B. Shen, “Dung beetle optimizer: a new meta-heuristic algorithm for global optimization,” *Journal of Supercomputing*, vol. 79, no. 7, pp. 7305–7336, May 2023, doi: 10.1007/s11227-022-04959-6.
- [11] C. Mai, L. Zhang, X. Chao, X. Hu, X. Wei, and J. Li, “A novel MPPT technology based on dung beetle optimization algorithm for PV systems under complex partial shade conditions,” *Sci Rep*, vol. 14, no. 1, Dec. 2024, doi: 10.1038/s41598-024-57268-8.
- [12] Q. Li, H. Shi, W. Zhao, and C. Ma, “Enhanced Dung Beetle Optimization Algorithm for Practical Engineering Optimization,” *Mathematics*, vol. 12, no. 7, Apr. 2024, doi: 10.3390/math12071084.
- [13] Q. Wu, H. Xu, and M. Liu, “Applying an improved dung beetle optimizer algorithm to network traffic identification,” *Computers, Materials and Continua*, vol. 78, no. 3, pp. 4091–4107, 2024, doi: 10.32604/cmc.2024.048461.
- [14] Koh, H. Y., Sequin, C. H., & Gray, P. R. (1990). OPASYN: a compiler for CMOS operational amplifiers. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 9(2), 113–125. <https://doi.org/10.1109/43.46777>
- [15] S. Asaithambi and M. Rajappa, “Swarm intelligence-based approach for optimal design of CMOS differential amplifier and comparator circuit using a hybrid salp swarm algorithm,” *Review of Scientific Instruments*, vol. 89, no. 5, May 2018, doi: 10.1063/1.5020999.
- [16] M. A. Valencia-Ponce, E. Tlelo-Cuautle, and L. Gerardo de la Fraga, “On the sizing of cmos operational amplifiers by applying many-objective optimization algorithms,” *Electronics (Switzerland)*, vol. 10, no. 24,

- Dec. 2021, doi: 10.3390/electronics10243148.
- [17] Acar Vural, Revna & Erkmen, Burcu & Bozkurt, Ufuk & Yildirim, Tülay. (2013). CMOS Differential Amplifier Area Optimization with Evolutionary Algorithms. World Congress on Engineering and Computer Science, WCECS 2013. 2. 666-670.
- [18] R. A. Vural and T. Yildirim, "Analog circuit sizing via swarm intelligence," *AEU - International Journal of Electronics and Communications*, vol. 66, no. 9, pp. 732–740, Sep. 2012, doi: 10.1016/j.aeue.2012.01.003.
- [19] Revna acar vural. "Particle swarm optimization for electronic circuit design automation" Ph.D. Dissertation, Yildiz Technical University Graduate School of Natural and Applied Sciences, 2011.
- [20] Ratan, S., Mondal, D., Kumar, C., Kumar, A., Jarwal, D. K., Mishra, A. K., Kar, R., & Jit, S. (2018). Optimization of Area of CMOS Differential Amplifier Using Modified PSO Algorithm. 2018 3rd International Conference for Convergence in Technology (I2CT), 1–6. <https://doi.org/10.1109/I2CT.2018.8529407>
- [21] R. A. Thakker, M. S. Baghini, and M. B. Patil, "Low-Power Low-Voltage analog circuit design using hierarchical particle swarm optimization," in *Proceedings: 22nd International Conference on VLSI Design - Held Jointly with 7th International Conference on Embedded Systems*, 2009, pp. 427–432. doi: 10.1109/VLSI.Design.2009.14.
- [22] Mushahhid Majeed, M. A., & Rao, P. S. (2017). Optimization of CMOS Analog Circuits Using Grey Wolf Optimization Algorithm. 2017 14th IEEE India Council International Conference (INDICON), 1–6. <https://doi.org/10.1109/INDICON.2017.8487592>
- [23] K. B. Maji, B. P. De, R. Kar, D. Mandal, and S. P. Ghoshal, "CMOS Analog Amplifier Circuits Design Using Seeker Optimization Algorithm," *IETE J Res*, vol. 68, no. 2, pp. 1376–1385, 2022, doi: 10.1080/03772063.2019.1649207.
- [24] Mallick, S., Sudhakar, K., Kar, R., Mandal, D., & Ghoshal, S. P. CMOS analog amplifier circuit sizing using opposition based harmony search algorithm. 2016 International Conference on Communication and Signal Processing (ICCSP), 1589–1593. <https://doi.org/10.1109/ICCSP.2016.7754428>.
- [25] S. Mallick, R. Kar, S. P. Ghoshal, and D. Mandal, "Optimal sizing and design of CMOS analogue amplifier circuits using craziness-based particle swarm optimization," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 29, no. 5, pp. 943–966, Sep. 2016, doi: 10.1002/jnm.2155.
- [26] Prajapati, P. P., & Shah, M. v. (2020). Automatic sizing of CMOS-based analogue circuits using Cuckoo search algorithm. *Int. J. Intelligent Systems Technologies and Applications*, 19(2), 125–140.
- [27] P. P. Prajapati, "Computer aided cmos based analog circuit design.", Ph.D. Dessertation, Gujarat Technological University, 2019.
- [28] P. P. Prajapati, A. J. Kshatriya, D. N. Patel, S. K. Gonsai, H. B. Tank, and K. R. Sheth, "Comparative analysis of meta heuristics algorithm for differential amplifier design," *Bulletin of Electrical Engineering and Informatics*, vol. 12, no. 6, pp. 3395–3401, Dec. 2023, doi: 10.11591/eei.v12i6.6153.