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Enhancing Intermediate DC Modules Voltage Control in Unified Power Quality Conditioner (UPQC) : Comparative Studies of Nonlinear Controllers

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Abstract: - Proportional Integral (PI) controllers are commonly used in the intermediate DC module voltage control of the shunt Active Power Filter (APF) side of the Unified Power Quality Conditioner (UPQC) to regulate the DC voltage, which in turn determines the amount of current compensation. Two nonlinear controllers are introduced for replacing the PI controllers to reduce the effects of overshooting and jitter signals generated by the PI controllers as well as to stabilize the intermediate DC module voltage. Firstly, the second-order sliding mode controller is designed to replace the PI controller based on the Super-Twisting Algorithm (STA) sliding mode controller, and this is followed by the non-linear controller of Anti Disturbance Rejection Controller (ADRC) designed to replace the PI controller based on the anti disturbance control principle. The Simulink module in MATLAB software is used to build the UPQC under the three models of non-linear controllers of PI, STA sliding mode, and ADRC based on the similar case study of voltage disturbances. The implementation of ADRC as a controller at the shunt APF side of UPQC has been shown to minimize output DC voltage fluctuation and provide the most stable DC voltage during voltage disturbances. In terms of the current response compensation, the ADRC controller responds faster and produces less overshoot than the nonlinear STA sliding mode controller. This demonstrates that the ADRC controller offers superior performance in terms of both voltage stability and current response compensation compared to traditional controllers. Its ability to minimize output DC voltage fluctuation, provide stable DC voltage, faster response times and reduced overshoot during disturbances makes it a highly effective choice for UPQC applications.

Keywords: *Unified Power Quality Conditioner (UPQC), Proportional Integral Controller Theory, Shunt Active Power Filter, Intermediate DC Modules, Anti Disturbance Rejection Controller, Super-Twisting Algorithm, Sliding Mode Control.*

I. INTRODUCTION

Power quality problems in distribution network become more prevalent as microgrids become more widely used. In addition, due to the increasing usage of high-precision machinery and sensitive equipment in industry, the manufacturing sector is focusing more on maintaining power quality and hence raising the power quality standards for end users. The key strategy for resolving this issue is to continue using a range of power quality control devices to mitigate power quality problems.

There are various types of power quality control devices on the market that are used in distribution networks. The Static Var Compensator (SVC) is commonly employed to dynamically correct reactive power, instantaneous active power, and phase-to-phase power exchange [1-3]. However, the SVC is a simple device having limited compensation precision in power quality improvement. However, the use of a Static Synchronous Compensator (STATCOM) will be necessary for more precise control and compensation. STATCOM provides faster response and more accurate voltage regulation compared to SVC that makes it suitable for high-demand in power systems [4-5]. On the other hand, Active Power Filtering (APF) is generally utilized in power systems to handle two issues of reactive power compensation and harmonic current. APC is more effective than traditional static compensation methods of SVC and STATCOM because of its ability to

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track voltage and current disturbances precisely and dynamically [6–9]. The Dynamic Voltage Restorer (DVR) is a series APC connecting between grid and load that ensures a constant supply of electricity during voltage fluctuation [10–15].

Unified Power Quality Conditioner (UPQC) is an integrated power quality control device that simultaneously compensates for both voltage and current disturbances. UPQC consists of a capacitor at the DC link connecting between the series and shunt APFs [16]. This allows UPQC to provide a versatile solution for improving a wide range power quality problems such as harmonics, voltage sags, voltage swells, voltage fluctuation and flicker, unbalanced voltage conditions, excessive reactive power and power losses [17–20]. In UPQC, the shunt APF regulates the grid current, while the series APF compensates for the grid voltage. One of the main topics discussed in recent studies is the topology and control method of UPQC for successfully sustaining the mitigation of power quality problems. Basically, there are different topological structures of UPQC such as single-phase two-wire systems, three-phase three-wire systems, and three-phase four-wire systems [21-25]. A three-phase having three-wire system is customarily used in most cases. PI controller is frequently employed in the three-phase three-wire UPQC structure and its current compensation module is a tightly coupled with the multi-variable of nonlinear system. The three-phase three-wire UPQC has a weak dynamic anti-disturbance performance because of a poor dynamic reaction in the PI controller and is very sensitive to changes of disturbances.

In the implementation of UPQC using the intermediate DC modules voltage control, the commonly used control methods are PID control and sliding mode control. PID control is the earliest and most widely used, however it is not suitable for high-frequency AC control and is prone to steady state error. Zhengming et al. [26] utilized the fractional order PID controller in UPQC that has the advantages of flexible structure and wider control range. However, the process of digital discretization is more complex and requires more adjustments to be made to various parameters. On the other hand, the conventional sliding mode control is another technique of intermediate DC modules voltage control used in UPQC. However, it usually suffers from jittering signals that increases switching losses and causing electromagnetic interference. Zhijun et al. [27] used a neural network technique in a sliding mode controller to enhance its response speed of the controller, although the structure was more intricate. Yili et al. [28] introduced a sliding mode passive control to improve power quality. Nevertheless, the convergence law of sliding mode in this application is complex since it requires the implementation of additional control mechanisms.

Therefore, this paper presents a nonlinear controller of Anti Disturbance Rejection Controller (ADRC) to replace the PI controller in the intermediate DC control module on the shunt APF side of the UPQC, in order to stabilize the DC bus voltage value of the intermediate DC module. Subsequently, the effectiveness of the control effect produced by the nonlinear ADRC controller is verified by comparing with the Super-Twisting Algorithm (STA) sliding mode controller. The UPQC has been implemented in a three-phase power system model which includes nonlinear loads and voltage disturbances. The results have shown that the ADRC controller used in UPQC has an advantage in terms of resilience in maintaining stability during disturbances, compared to the results obtained by the UPQC using STA sliding mode and PI controllers.

II. IMPROVED UPQC SYSTEM BASED ON THE SECOND-ORDER SLIDING MODE CONTROLLER USING SUPER-TWISTING ALGORITHM

A three-phase three-wire UPQC was employed and the topology is shown in Figure 1. Three-phase grid power supply are recorded as V_{sa}, V_{sb}, V_{sc}. Common DC terminal, series injection transformer, series APF (SEF), shunt APF (SAPF), LC filter, and three-phase unbalanced nonlinear load module are the main parts of the device. The three-phase currents output at the power supply terminal are recorded as I_{sa}, I_{sb}, I_{sc}, respectively and the three-phase current output at the three-phase nonlinear load terminal are recorded as I_{La}, I_{Lb}, I_{Lc}, respectively. The three-phase voltage output at the load terminal are recorded as V_{La}, V_{Lb}, V_{Lc} respectively. C_{F1}, C_{F2} are the capacitance value of the intermediate DC module. V_{c1}, V_{c2} are the value of the voltage across the intermediate DC module capacitor.

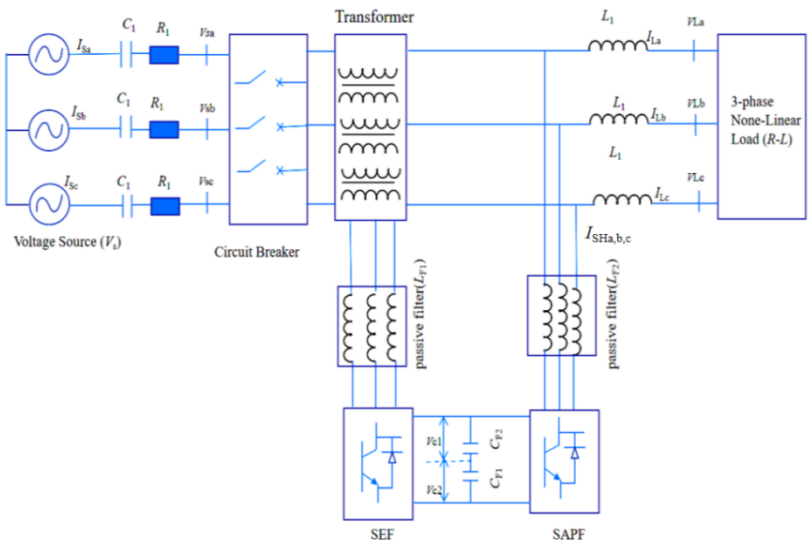

Figure 1.Three-phase three-wire of UPQC consisting of SEF and SAPF.

This UPQC topology is referenced from the literature [29]. Figure 2 shows the control diagram of the shunt APF side of the UPQC [30], and since the focus of this study is on the DC bus voltage controller, this module is mainly located in the shunt APF part of the UPQC. The ADRC and STA sliding mode controllers designed in this study are mainly applied to the DC control module in a ahunt APF. The part of the control diagram consisting of the blue coloured modules is the self-tuning filter integrated with the unit vector generator (STF-UVG) technique. The section consisting of the green coloured modules is the control flow of the ahunt APF. The phase angle of the fundamental wave component of the original grid-side voltage will be obtained in the STF-UVG. The intermediate DC module that used to make changes in this study is the PI controller for the orange coloured module shown in in Figure 2. From the figure, it can be seen that the STF-UVG output positive sequence component phase angle sin(ωt) and cost(ωt) of the blue coloured modules is given to the green coloured modules for coordinate conversion, which is used to obtain the final compensation current $I_{SHa,b,c}^{*}$ required by the SAPF.

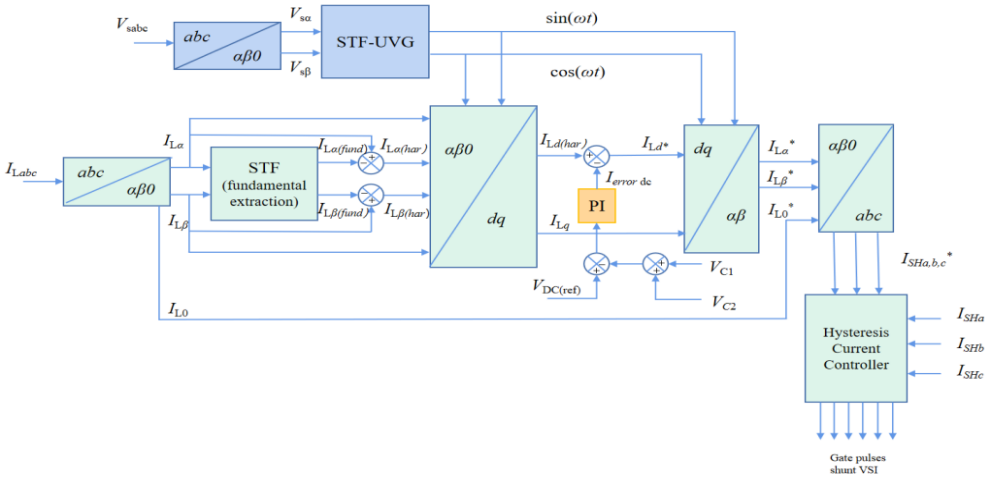

Figure 2. Control flow diagram of shunt APF in UPQC.

A. STA Sliding Mode Controller in SAPF Module of UPQC

The PI controller reacts sensitively that produces a significant overshoot when the load changes abruptly and this is insufficient to fulfill the system's criteria for sustaining the anti-disturbance stability. Sliding mode control able to overcomes the system uncertainty and is robust to mitigate the disturbances which is widely used due to the simplicity of the algorithms and fast response time of the variable structure control system, as well as its immunity to external noise disturbances and parameter ingressions [31 – 33]. The output of the

control signal is prone to chattering and the conventional sliding mode control is a discrete control technique. Numerous specialists and academics have conducted in-depth study on the chattering issue brought on by the conventional sliding mode and have developed a number of chattering suppression techniques, including boundary layer method and approaching legislation. According to these study findings, second-order sliding mode control can both successfully decrease chattering as well as maintain the robustness of sliding mode control.

With the appropriate SAPF, reactive current and current harmonics may be adequately compensated in the three-phase three-wire UPQC system. The typical PI control approach used in the shunt terminal SAPF is derived as follows in order to appropriately compensate the current.

$$e_{v1} = V_{DC(ref)} - (V_{C1} + V_{C2}) \tag{1}$$

$$I_{DC} = K_{p(DC)} e_{v1} + K_{i(DC)} \int_0^t e_{v1} dt \tag{2}$$

V_{C1} is the actual terminal voltage value of the capacitor on the upper side of the intermediate DC terminal of the series-shunt APFs, and V_{C2} is the actual terminal voltage value of the capacitor on the lower side of the intermediate DC terminal of the series-shunt APFs. The voltage difference between the upper and lower terminals of the intermediate DC terminal capacitor is represented by e_{v2}, while the reference voltage and actual difference between the intermediate DC terminal is represented by e_{v1}. I_{DC} is the compensation current reference value calculated from the intermediate DC terminal. $K_{p(DC)}$, $K_{i(DC)}$ are proportional and integral coefficients when I_{DC} is controlled by PI controller. The specific control principle block diagram is shown in Figure 3.

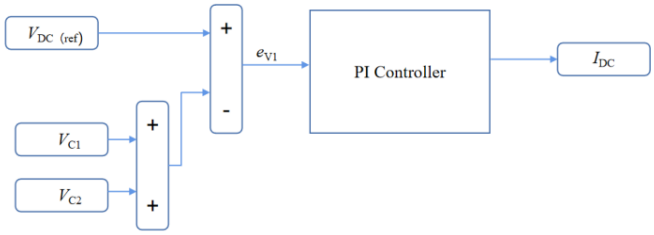

Figure 3. PI controller block diagram.

In this study, the intermediate DC module of STA sliding mode controller is used to replace the traditional PI controller in Figure 2. The The STA sliding mode control algorithm realizes the continuous control quantity in time by applying the discrete control rule to the high order effectively suppressing chattering [34]. The second-order STA sliding mode control algorithm a generally consists of two parts which is a continuous function on the first sliding mode surface set to a_1, and an integral in time over the second sliding mode surface set to a_2.

$$a = a_1 + a_2 \tag{3}$$

$$a_1 = -k_1 |s|^{\rho} sign(s) \tag{4}$$

$$a_2 = k_2 sign(s) \tag{5}$$

$$\text{sign}(s) = \begin{cases} 1, s > 0 \\ -1, s < 0 \end{cases} \tag{6}$$

where, k_1 is the coefficient of the exponential term and k_2 is the coefficient of the integral term. $k_2>0$, $sign$(s) is a sign function, and ρ is the coefficient of the exponent term. Equation (5) occurs as a time integral in the second-order STA sliding mode control law instead of directly affecting control law a since it is a discontinuous high-frequency switching quantity. On the basis of this idea, the chattering phenomena in the sliding mode control is eliminated and the continuous control signal is thus obtained.

In order to achieve system convergence within a limited time, ρ in equation (4) should satisfy $0<\rho\leq0.5$, and the value of ρ chosen in this study is 0.5. The sliding mode variables s is as follows.

$$s = e_{v1} = V_{DC(ref)} - (V_{C1} + V_{C2}) \tag{7}$$

The final STA sliding mode control law is obtained as shown in equation (8), and the controller design is shown in Figure 4 and Figure 5.

$$I_{DC} = u = k_p |s|^{1/2} sign(s) + \int k_i sign(s) dt \tag{8}$$

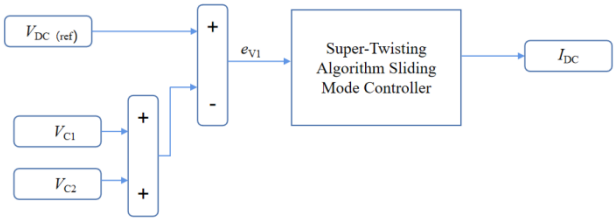

Figure 4. The design of STA sliding mode controller.

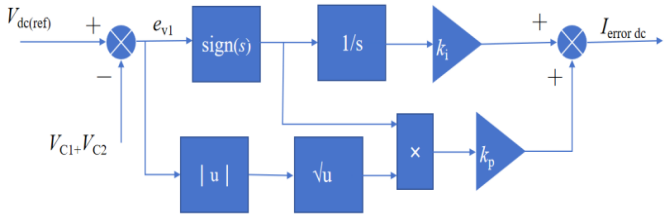

Figure 5. STA sliding mode controller module diagram.

B. Proof of System Stability

The Lyapunov function is frequently employed for verification during examining the stability of the system that utilizes the automated control approach. It is important to build a positive definite function $V=s^2/2$, where s is the sliding mode variable, which is obtained from equation (11) in order to make the system satisfy the accessibility requirement of sliding mode control $\dot{s}s<0$.

$$V = s\dot{s} = s\left[\dot{V}_{DC(\text{ref})} - \left(\dot{V}_{C1} + \dot{V}_{C2}\right)\right] \tag{9}$$

$$e_{v1} = V_{DC(ref)} - (V_{C1} + V_{C2}) \tag{10}$$

When $s>0$, that is, $V_{DC\ (ref)}>V_{C1}+V_{C2}$ and $i_1+i_2>0$. Hence, equation (12) satisfies $V<0$. When $s<0$, that is, $V_{DC\ (ref)}<V_{C1}+V_{C2}$ and $i_1+i_2<0$. Therefore, equation (12) satisfies $V<0$. As a results, equation 12 will satisfies the Lyapunov stability condition and the second-order STA sliding mode controller is inflicting a stable system.

III. IMPROVED UPQC SYSTEM BASED ON ACTIVE DISTURBANCE REJECTION CONTROLLER

A. Active Disturbance Rejection Control (ADRC) Design

The sudden load changes may cause the PI controller responds sensitively and easily forms a large overshoot which cannot meet the UPQC requirements for anti-disturbance stability. The system state and unknown disturbance can be estimated using active disturbance rejection control (ADRC) technology in real time, whereby the system's active disturbance rejection control law can be obtained by combining nonlinear state errors. This technology eliminates the need for a control model and enables accurate compensation for disturbances to be tracked quickly [29-33]. The nonlinear ADRC controller consists of three parts described as follows. The tracking

differentiator (TD) mainly arranges the transition process for the reference signal. Extended State Observer (ESO) is the vital control part of ADRC. The ADRC regards all uncertainties and disturbances as a whole, and uses ESO to observe these disturbances. The non-linear state error feedback control law (NLSEF) primarily distinguishes between the reference signal, differential signal, and state signal produced by TD and ESO before performing a nonlinear combination to determine the error feedback control amount.

In this study, the intermediate DC module of ADRC controller is used to replace the traditional PI controller in Figure 2. The control principle block diagram of the ADRC controller is shown in Figure 6. The Object module is the controlled target value.

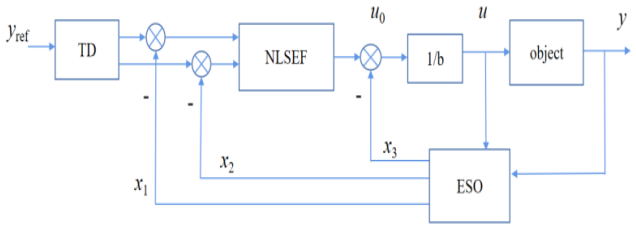

Figure 6. ADRC control principle block diagram.

In the three-phase three-wire UPQC system, the ADRC controller is applied in the SAPF module with the voltage input of the intermediate DC capacitor link and the current IDC output as shown in Figure 7 and Figure 8.

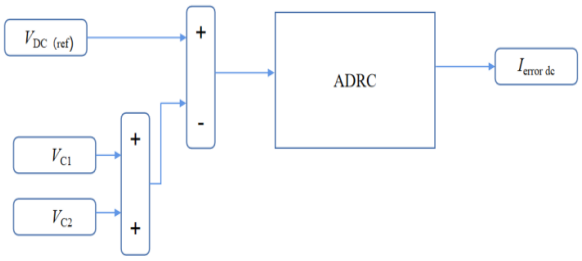

Figure 7. Input and output of ADRC controller.

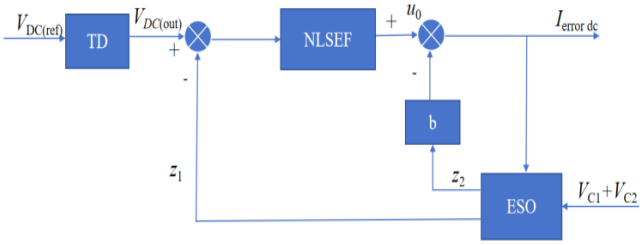

Figure 8. ADRC controller diagram.

1) Tracking Differentiator (TD) Design

The design of TD mainly tracks and transit or change the voltage output value of the intermediate DC link, V_{DC}, from the reference voltage output value, $V_{DC\ (ref)}$.

$$\begin{cases} e_0 = V_{DC(out)} - V_{DC(ref)} \\ \dot{V}_{DC(out)} = \beta_0\, fal(e_0, \alpha_0, \delta_0) \end{cases} \tag{11}$$

where, e_0 is the error value of the intermediate DC voltage V_{DC}, and *fal* is the continuous idempotent function with a linear segment. The specific expression of this function is shown in equation (12).

$$fal(e_0,\alpha_0,\delta_0)=\begin{cases}|e_0|^{\alpha_0}sign(e_0), |e_0|>\delta_0\\ e_0/\delta_0^{1-\alpha_0}, |e_0|\le\delta_0\end{cases} \tag{12}$$

where, α_0 is the exponent value, δ_0 is the base of the exponential function, and *sign* is the signal function. The procedure to determine the α, β and δ_0 will be explained in the following subsection that is similarly applied for the NLSEF and ESO.

2) The Non-Linear State Error Feedback Control Law (NLSEF) Design

NLSEF mainly performs perturbation suppression and abatement. Based on the errors of the given signal and the differentiation of the signal derived from the TD, with the system outputs, output derivatives observed by the ESO, and thus control and disturbance compensation.

$$\begin{cases} e_1=V_{DC(\text{out})}-z_1\\ u_0=\beta_1 fal(e_1,\alpha_1,\delta_1)\end{cases} \tag{13}$$

where, z_1 is the observed value of V_{DC} and u_0 is the output of the NLSEF.

3) The Extended State Observer(ESO) Design

ESO mainly estimates the real-time action value of disturbances inside and outside the system, and gives compensation in the feedback, and eliminates the effect of disturbances with compensation, thus having the effect of anti-interference. z_1 is the tracking signal and z_2 is the total system interference estimate.

$$\begin{cases} e_2=z_1-(V_{C1}+V_{C2})\\ \dot{z}_1=z_2-\beta_2 fal(e_2,\alpha_2,\delta_2)+bu(t)\\ \dot{z}_2=-\beta_3 fal(e_2,\alpha_2,\delta_2)\end{cases} \tag{14}$$

where, $u(t)$ is the perturbation compensation term, and the specific compensation equation is shown in Equation 15.

4) Disturbance Compensation Process

In equation (15), *u0* is the given value of the compensation voltage, and $u(t)$ is the actual given value of the voltage after compensation. z_2 in equation (15) is the same as in equation (14). bz_2 is the amount of perturbation.

$$u(t)=u_0-bz_2 \tag{15}$$

B. Parameters Selection in the ADRC Controller

The nonlinear function *fal* used in TD, ESO, and NLSEF is a continuous idempotent function with a linear segment. *a* as the coefficient of the exponential term in the *fal* function generally has the following properties according to the exponential function properties. When $\alpha<1$, it has the characteristics of small error large gain and large error small gain, which can reduce the system steady state error, improve dynamic performance, improve disturbance suppression ability, and avoid the system to produce steady state high-frequency jittering signals at the same time.

Therefore, the selection principles of ESO parameters used in *fal* function are elaborated in the following procedure.

(1) Select α_2 with the value of 0.9 that is between the specified range of 0 and 1.

(2) Choose 0.01 as the practical value for δ_2. The δ_2 represents as the width of linear interval near to the origin which is related to the error range of a system. Generally, the range is $0.0001\le\delta_2\le1$. However, the δ_2 smaller than 0.0025 may cause high-frequency fluctuations increasing in a system. However, a large value of δ_2 may cause failure of the nonlinear feedback control.

(3) Select the values of β_2 and β_3 according to the tracking performance of ESO. Albeit, large values of β_2 and β_3 are beneficial to improve the tracking speed of ESO. However, it is easy to cause oscillation and overshoot at the output. Usually, the value of β_3 is in the order of 1~2 larger than the magnitude of β_2.

The aforementioned procedure of is similarly applied to choose the best parameters of α, δ, and β required by the *fal* function used in the TD and NLSEF modules.

IV. RESULTS AND DISCUSSION

The UPQC system shown in Figure 1 is used as a case study to verify the robustness of ADRC and STA sliding mode controller to improve the performance of SAPF controller shown in Figure 2. The electrical components parameters of the three-phase three-wire UPQC system used in the case study are shown in Table 1.

TABLE 1. Electrical parameters used in the UPQC.

Parameters	Value
V_s	100V
L_1	10mH
R-L	100Ω-100mH
R_1-C_1	7Ω-200uF
LF_1	10mH
LF_2	10mH
C_{F1}-C_{F2}	3300uF

The simulation time of 2s is used to observe the performance of UPQC that is connected to a nonlinear load. In Figure 1, the voltage source, V_s, is supplying base case value of 100V during the beginning operation of the system, which is then the voltage V_s falls to 0.7 p.u. from its base case V_s value at the operating time of 1s due to the commencement of voltage sag. Simultaneously, UPQC mitigates the voltage dips generated by V_s by maintaining the reference value of 100V and restores the voltage V_L on the load side until the end of the voltage dips at 1.5 s. The V_s voltage waveform is shown in Figure 9. The performance of UPQC in mitigating the voltage sag can be evaluated by comparative studies on the effects of PI controller, STA sliding mode controller and ADRC controller implemented in the SAPF. The proportional coefficient, *P*, of 0.3, and the integral coefficient, *I*, of 2 were set for the *PI* controller used in the SAPF of UPQC. On the other hand, k_i =10, and k_p=0.5 are the coefficients specified for the STA sliding mode controller used in the SAPF of UPQC. In the SAPF using the ADRC controller for UPQC, the parameters setting are a_0=0.9, a_0=a_1=a_2=0.9, β_0=200, δ_0=δ_1=δ_2=0.01, β_1=1.6, β_2=400, β_3= 4000, *b*=690.

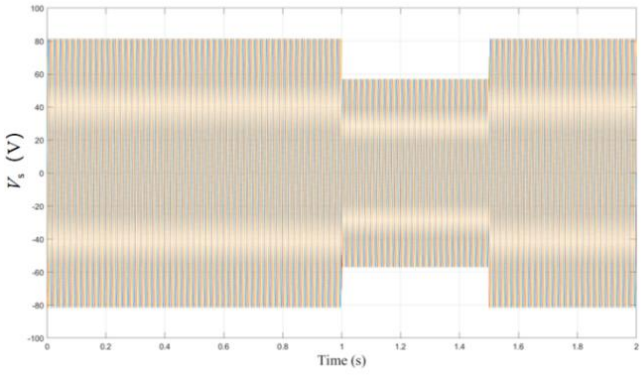

Figure 9.**Waveform of grid-side voltage V_s.**

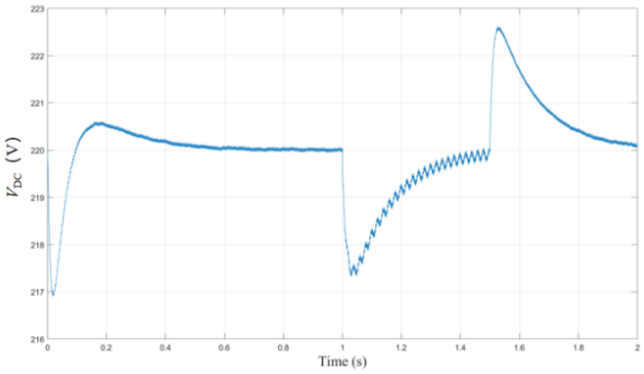

Figure 10. V_{DC} **from the output of intermediate DC module of PI controller used in SAPF-UPQC**

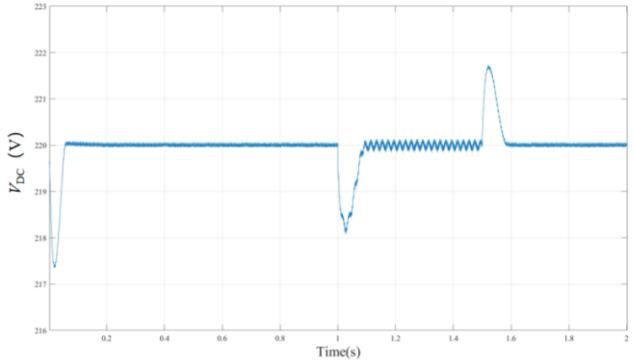

Figure 11. V_{DC} **from the output of intermediate DC module of STA sliding mode controller used in SAPF-UPQC.**

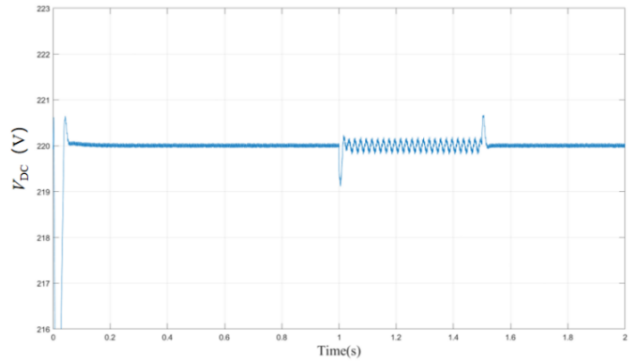

Figure 12. V_{DC} **from the output of intermediate DC module of ADRC controller used in SAPF-UPQC.**

Figures 9, 10 and 11 show the comparison results of V_{DC} coming from the output of intermediate DC modules of PI controller, STA sliding mode controller and ADRC controller, respectively. In Figure 9, it can be seen that the V_{DC} output of intermediate DC module for PI basically reaches its stability until the time interval of 1s. A downward voltage transient of V_{DC}=217.7V can be seen at 1s affected by the commencement of voltage sag in V_s. This is followed by the negative oscillation representing the sawtooth voltage waveform of V_{DC} slowly rising from 217.5V until 220V between the time interval of voltage sag occurrence that is from 1s until 1.5s. A sudden increase of upward voltage transient of V_{DC}=222.5V occurred at 1.5s during the end of voltage sag, and subsequently the V_{DC} is slowly declining until it reaches to 2s. The results has shown that the PI controller failed to stabilize during voltage sag mitigation owing to a poor response of V_{DC} to recover or sustain at 220V, which was impacted by the downward and upward voltage transients.

It contradicts the V_{DC} findings obtained by the STA sliding mode controller and the ADRC controller utilized in the SAPF of UPQC. The fast recovery response to maintain the V_{DC} at 220V after the downward voltage transient

of V_{DC}=218V at 1s and the upward voltage transient of V_{DC} =221.7V at 1.5s, indicates that the STA sliding mode is stable in mitigating the voltage sag.

On the other hand, the ADRC controller also exhibits stability in mitigating voltage sag by reflecting on the V_{DC} result. This is supported by its fast recovery response by ensuring that the V_{DC} remains at 220V after the downward voltage transient of V_{DC}=219V at 1s and the upward voltage transient of V_{DC} =220.6V at 1.5s. Furthermore, the ADRC controller provides much better stability than the PI and STA sliding mode controllers by producing a more refine sawtooth voltage waveform of V_{DC}. This is further proven by observing the downward and upward voltage transients of V_{DC} produced by the ADRC controller, which are lower than those produced by the PI and STA sliding mode controllers.

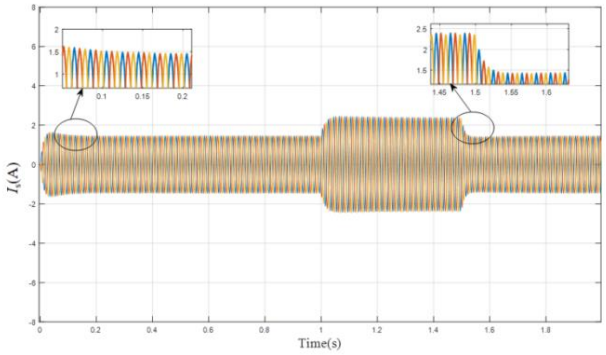

Figure 13. I_S with the impact of voltage sag with non-linear load mitigated by UPQC using PI controller based SAPF.

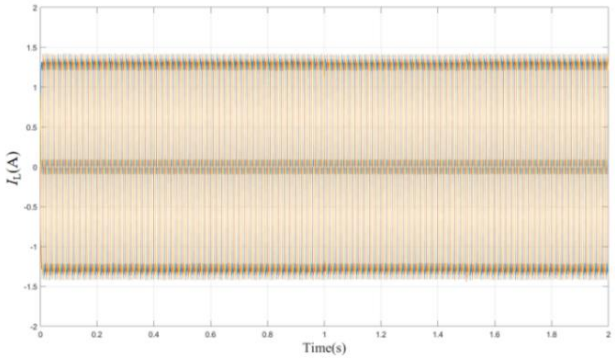

Figure 14. Consistent I_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using PI controller based SAPF.

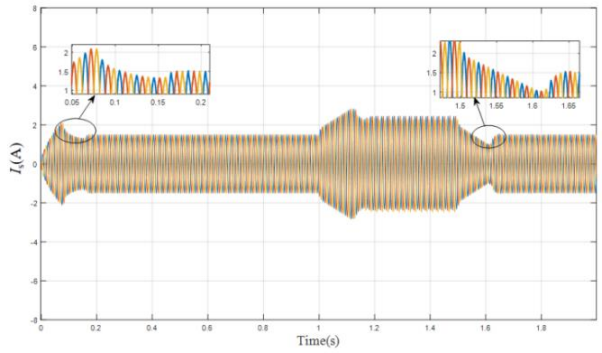

Figure 15. I_S with the impact of voltage sag with non-linear load mitigated by UPQC using STA sliding mode controller based SAPF.

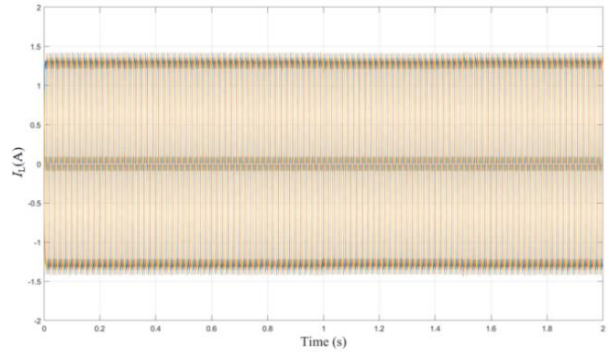

Figure 16. Consistent I_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using STA sliding mode controller based SAPF.

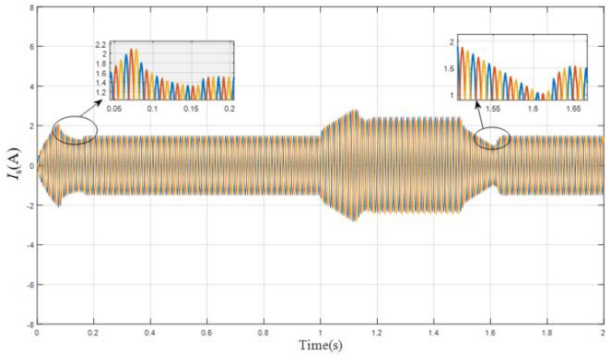

Figure 17. I_S with the impact of voltage sag with non-linear load mitigated by UPQC using ADRC controller based SAPF.

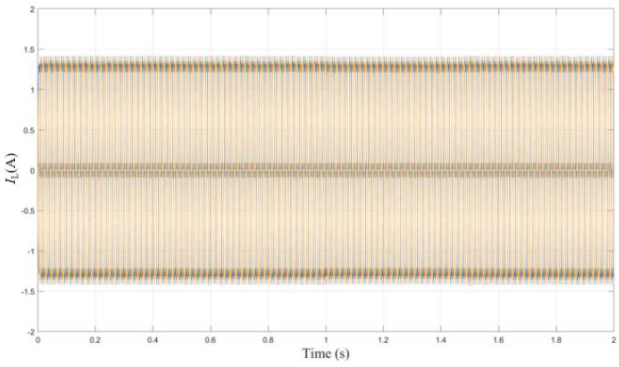

Figure 18. Consistent I_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using ADRC controller based SAPF.

Figures 13, 15, and 17 show the changes in source current I_s caused by the voltage sag and non-linear loads which are mitigated by the PI, STA sliding mode, and ADRC controllers, respectively. The implementation of the three intermediate DC modules have caused instability and delayed response at the beginning and end of the voltage sag mitigation at 1s and 1.5s, respectively. However, the implication of I_s has no effect on the load current, I_L, which remains at 1.4A due to the efficacy of the three intermediate DC modules in mitigating voltage sag during the time span from 1s to 1.5s as shown in Figures 14, 16 and 18.

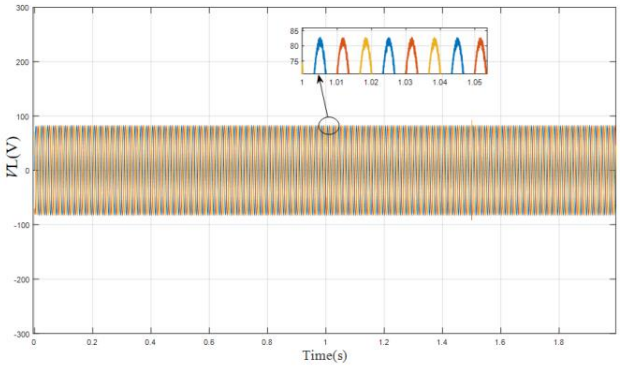

Figure 19. Consistent V_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using PI controller.

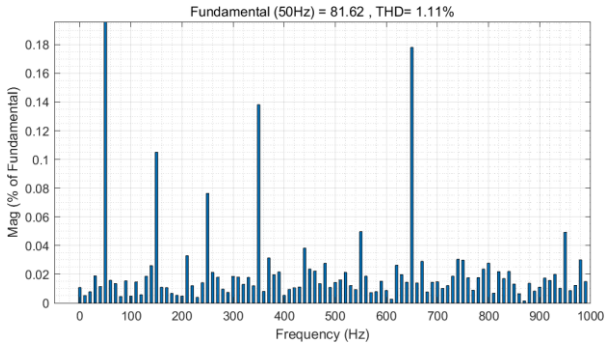

Figure 20. Harmonic analysis of V_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using PI controller.

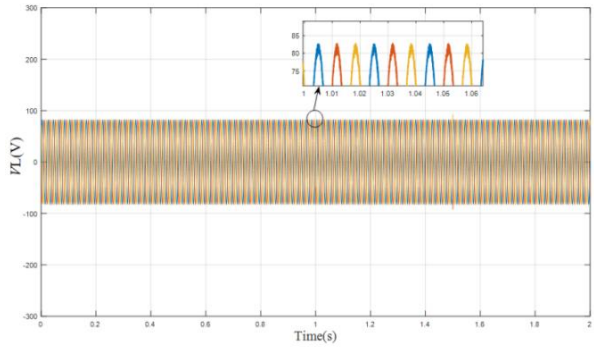

Figure 21. Consistent V_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using SAPF-STA sliding mode controller.

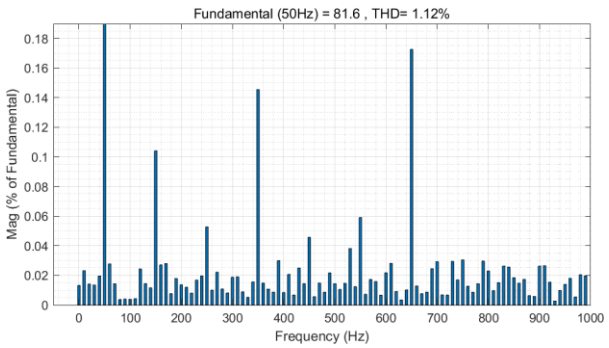

Figure 22. Harmonic analysis of V_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using SAPF-STA sliding mode controller.

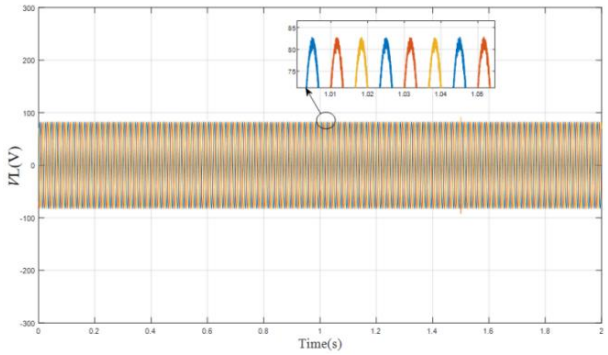

Figure 23. Consistent V_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using SAPF-ADRC controller.

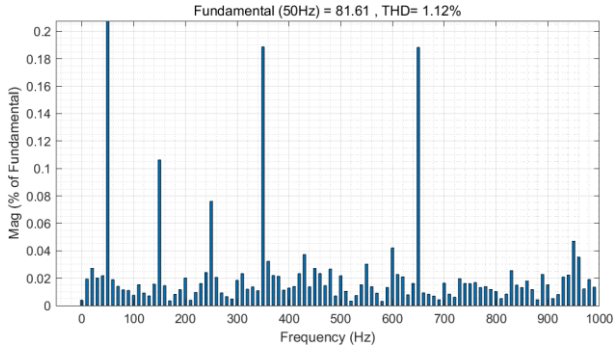

Figure 24. Harmonic analysis of V_L subject to the voltage sag mitigation with non-linear load performed by the UPQC using SAPF-ADRC controller.

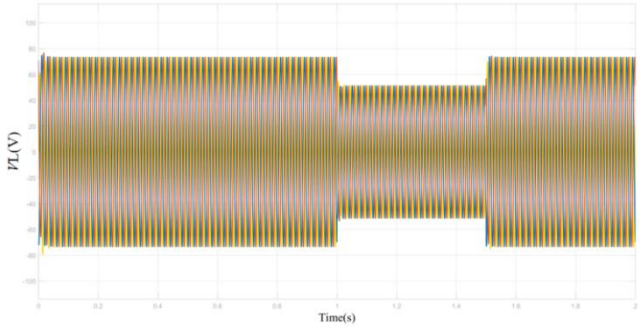

Figure 25. Consistent V_L subject to the voltage sag mitigation without UPQC.

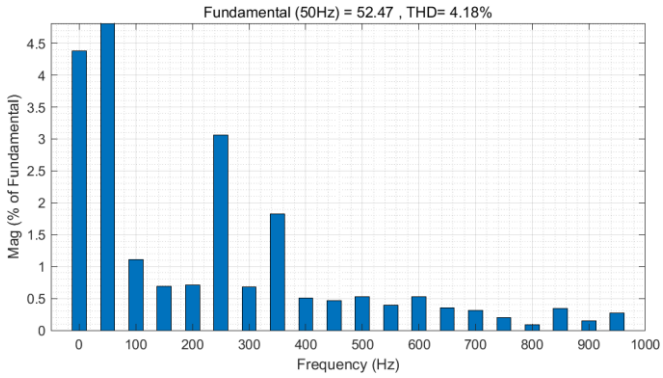

Figure 26. Harmonic analysis of V_L subject to the voltage sag mitigation without UPQC.

Figures 19, 21, and 23 show a consistent load voltage, V_L, of 83V subject to the voltage sag mitigation during the time interval from 1s to 1.5s performed by the UPQC which is effectively controlled by the SAPF with PI, STA

sliding mode, and ADRC controllers, respectively. In addition, Figures 20, 22, and 24 show the total harmonic distortion (THD) investigations were carried out on the five cycles of V_L starting from 1.2s, subject to the voltage sag mitigation performed by the UPQC with SAPF controlled by the three intermediate DC modules. The results illustrate that the magnitude and pattern of spectrum frequency for V_L are relatively similar for all the three cases of intermediate DC modules. Specifically, it signifies that the PI controller reduces the THD of V_L to 1.11% which is very similar to the 1.12% THD of V_L reduced by the STA sliding mode and ADRC controllers. When UPQC is not used for compensation, the load-side output voltage waveform V_L is shown in Figure 25. At this time, the load-side voltage harmonic THD value is 4.18.

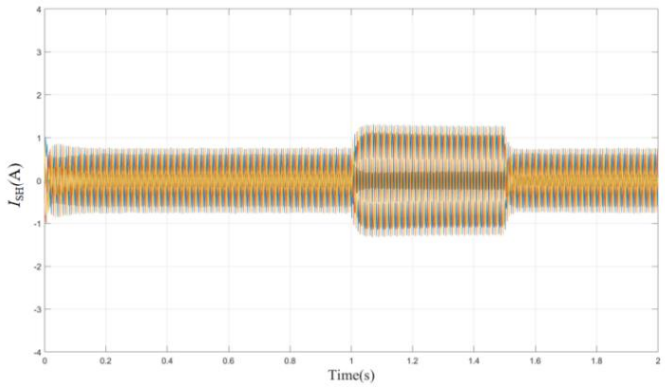

Figure 27. Result of I_{SH} for load current compensation performed by the UPQC using SAPF-PI controller.

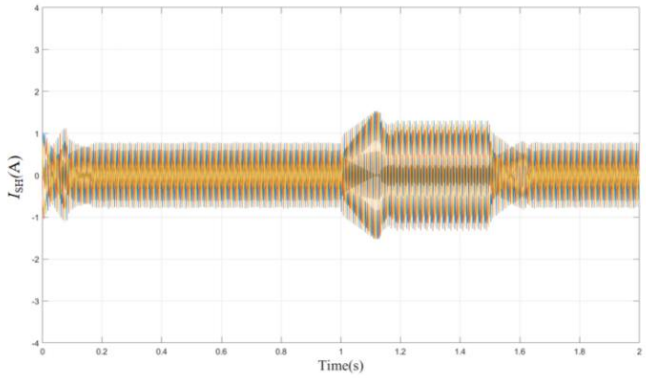

Figure 28. Result of I_{SH} for load current compensation performed by the UPQC using SAPF-STA sliding mode controller.

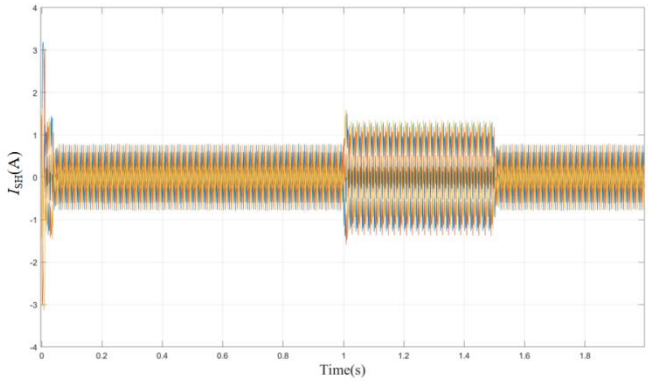

Figure 29. Result of I_{SH} for load current compensation performed by the UPQC using SAPF-ADRC controller.

Figures 27, 28 and 29 show the waveform of compensation current injected, I_{SH}, into the load side by the UPQC through SAPF using the three types of intermediate DC modules. Figure 27 depicts the injected current I_{SH}, which is utilized to compensate the load current within 0.5s when the voltage sag occurs between 1s and 1.5s. The usage of the PI controller in SAPF has led UPQC to respond slowly for I_{SH} to begin compensating at 1s and a delay for I_{SH} to stop compensating the load current that exceeds 1.5s. In Figure 28, the STA sliding mode controller employed in SAPF has caused instability in the UPQC operation, resulting in a longer time of 0.6s for I_{SH} to compensate the load current starting from 1s until 1.6s during the occurrence of a voltage sag. This implies that the I_{SH} takes longer time to compensate for load current than the UPQC does with SAPF based PI and ADRC controllers shown in Figures 27 and 29, respectively. Furthermore, Figure 28 shows that instability of I_{SH} significantly delayed the response to compensate load current beginning at 1s and considerably slowed the response to stop load current compensation until it reached 1.6s. Figure 29 shows the efficient response of I_{SH} in compensating the load current through the stability performance of UPQC assisted by the SAPF based ADRC controller. The I_{SH} has a substantially faster response and stability than I_{SH} produced by the UPQC that employs SAPF based on PI and STA sliding mode controllers shown in Figures 27 and 28, respectively. Due to the fact that the ADRC controller has a significant impact on the stability performance of UPQC, there is a minor overshoot on I_{SH} having 1.5A with a very short time occurring at the beginning of the load current compensation which is 1s, and it ends effectively at 1.5s as shown in Figure 29. The result findings conclude that the ADRC controller is an effective intermediate DC module used for improving the performance of SAPC based UPQC by providing stability and an effective response of I_{SH} in contrast to UPQC that uses SAPC based on the PI and STA sliding mode controllers.

V. CONCLUSION

The effectiveness of the shunt APF (SAPF) side of UPQC in mitigating power quality problems and improving grid stability has been evaluated using three intermediate DC modules of non-linear controllers which are the Proportional Integral (PI), Super-Twisting Algorithm (STA) sliding mode, and Anti Disturbance Rejection Controller (ADRC). The performance comparison of UPQC employing the three intermediate DC modules of non-linear controllers yielded the following findings.

(1) During the voltage sag mitigation, the ADRC controller based SAPF used in the UPQC produces the smallest oscillation for the V_{DC} output compared to the results obtained from the UPQC using SAPF with PI and STA sliding mode controllers.

(2) During the source current, Is, oscillation caused by the voltage sag and nonlinear loads, the three intermediate DC modules of non-linear controllers used in the SAPF of UPQC effectively compensate and mitigate the disturbances of load current, I_L, and load voltage, V_L, respectively.

(3) During the voltage sag mitigation, the PI and STA sliding mode controllers in SAPF have delayed the UPQC to start and to stop injecting the I_{SH} for load current compensation, as compared to the rapid compensation of I_{SH} performed by the ADRC controller. However, it was discovered that the ADRC controller produced a small overshoot of I_{SH} at the beginning of load current compensation. Therefore, it can be regarded acceptable due to its insignificant impact on the system.

As a compendium, the ADRC controller provides better performance in terms of stability and response time compared to the PI and STA sliding mode controllers used in the SAPF of UPQC. This signifies that the use of the ADRC controller enhances the effectiveness of UPQC in mitigating power quality problems.

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