[1]Vinayak Gaikwad,
[2]Dr. Prerna Goswami

Interoperability of Photovoltaic & Energy Storage Using a Modern Structure of an NPC Inverter with Enhanced Control Approach

Journal of Electrical Systems

Abstract: - This article presents a new approach to integrate Photovoltaic (PV) systems with energy storage using a 3-level Neutral Point Clamped (NPC) inverter in a grid-connected setup. The key innovation lies in the development of an extended unbalanced 3-level vector modulation scheme, capable of generating the required AC voltage even in the presence of unbalanced DC voltage conditions. The design methodology & conceptual framework for this modulation scheme are discussed in detail. Additionally, a novel control strategy is presented to control power flow between the solar PV array, battery storage, & the grid, while also ensuring maximum power point tracking (MPPT) operation for the PV system. The performance of the this propose method is evaluated through MATLAB simulations, considering different scenarios such as battery charging/discharging under varying solar irradiation conditions.

Keywords: Energy/ Battery Storage, PV, Space Vector Modulation (SVM), 3-level inverter, NPC inverter

I.INTRODUCTION

Renewable energy (RE) sources, including solar & wind generation systems, are becoming more appealing alternatives to conventional generators [1, 2] due to the worldwide natural resource scarcity & climate change associated with conventional power production. APE systems are vital for the harnessing & growth of RES. Power electronic systems serve an important purpose in solar PV & wind energy installations by ensuring that all of the electricity generated by the source has been used. [3]-[5]. Single-stage & double-stage translation are two popular electronic power designs used in 3-phase systems for transferring energy generated from renewable sources to the grid.

It is usual practice to employ a double-stage conversion process in conventional PV systems. This procedure involves a DC/DC converter & an inverter. The PV array is able to achieve MPPT with this configuration, and it also generates sufficient V_{dc} for the DC/AC inverter. On the other hand, this method requires the utilizations of two converters, which results in an increase in both expense and complexity [1-3]. Single-stage connections, on the other hand, are more expensive & more efficient than multi-stage connections, but they require more complicated control techniques. A 3-phase, single-stage construction that uses a VSC is an industry standard architecture for applications requiring significant power, such as grid-interfaced PV systems [4].

One of the most significant difficulties associated with RES is the fact that they are unpredictable & subject to fluctuations. These issues can be solved by integrating grid-connected RE systems with BES, which also improves the flexibility of the system during regulation & the stability of the network [5]. In most cases, different converters are utilized for the purpose of charging & discharging batteries as well as converting DC to AC energy.

This results in additional expenses & greater complexity. The author of this article suggests a novel approach, which is a 3-phase solar PV system that is connected to the grid & has battery storage & uses a single 3-level converter. As a result of this converter's capacity to perform MPPT, control the current on the AC side, & manage battery charging & discharging, it is able to reduce costs, improve efficiency, & enhance the controllability of power transfer [6].

After that, the other parts of this article are structured as follows: In the section II, the structure of a 3-level inverter & the voltage control that is associated with it are described. The topology that has been developed for integrating solar PV & Energy storage is shown in Section III, along with the control mechanisms that are linked with it. In

[1] *Corresponding author: Department of General Engineering, Institute of Chemical Technology, Mumbai, Mumbai. M.S., India

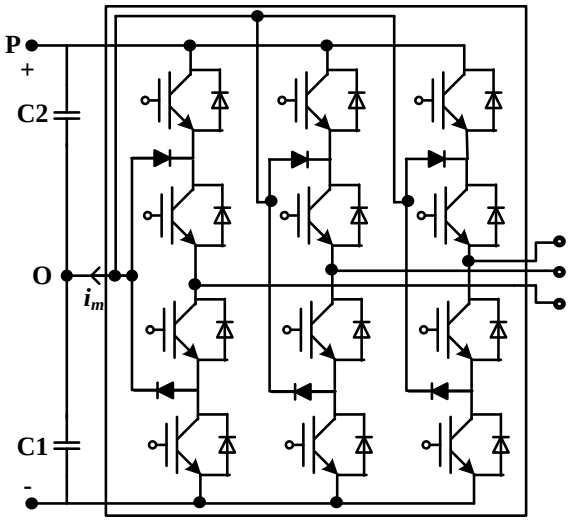
[2] Department of General Engineering, Institute of Chemical Technology, Mumbai, Mumbai. M.S., India

Section IV, the simulation & results of the suggested strategy & control network are discussed in detail. Last section the article comes to a conclusion remark of the research article.

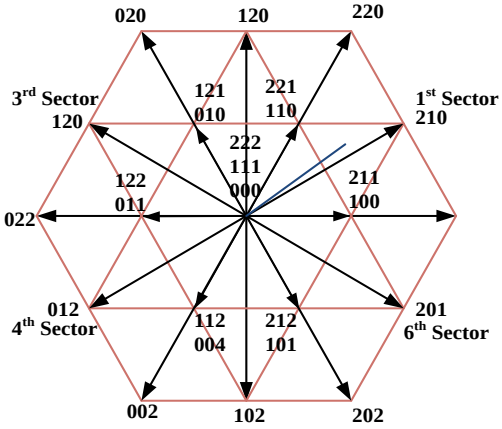
II.3-LEVEL INVERTER'S FRAMEWORK & CAPACITOR PARAMETERS ASPECTS

A. 3-Level Inverter

Since their incorporation in 1981 [6], [7], 3-level inverters have been used in a different application, which would include motor drives, FACTS, HVDC, as well as RE [7]. [8]. Fig. 1 (a) highlights a typical 3-phase, 3-level NPC inverter system. Two capacitors on the DC side generate the 3-level ac-side phase voltages. V_c is commonly assumed to be balanced as well because unbalanced V_c could indeed affect AC-side voltages & lead to unexpected behavior in the context of even-harmonic injection along with power ripple [7], [9]. Numerous publications [6], [7], [9], & [16] have discussed techniques for balancing these V_{cs} in various applications.



(a) Circuit configuration



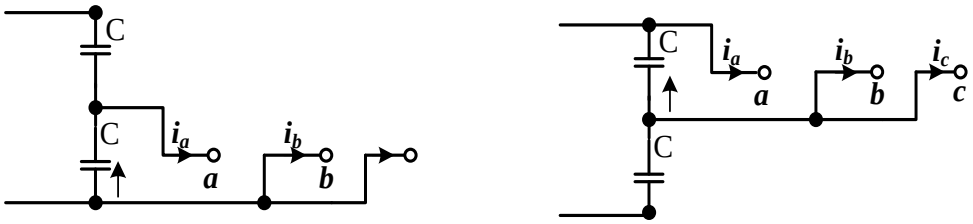
(b)A 3-level inverter space vector illustration for balanced DC-link capacitors.

Fig. 1. A typical 3-level inverter

B. Balanced Capacitors Voltage

Different approaches for balancing V_{cs} that use modulation methodologies such as SPWM or SVPWM have been recommended **[17].** In various SPWM applications, the balance of DC-link capacitors is achieved by incorporating the appropriate zero-sequence signal into the modulated signal [12-13], [16-18] Different strategies for balancing the V_c in the 3-level NPC inverter have been developed in the SPWM application sectors, considering the impacts of the switching on the V_c inside the vector space. Capacitor balancing can be accomplished with either authentic SPWM, emulated SPWM, or some combination of such [14-19].

Within the vector control concept, an inverter should ideally be capable of instantaneously generating the voltage output in response to the V_{ref} produced by the control scheme. However, due to the inverter's switch limitations, it cannot be guaranteed that any required vector will be produced; in reality, only a limited number of vectors (27 vectors for a 3-level inverter) will be derived. To address these limitations, any SVM arrangement, including SPWM or VSVPWM, generates the V_{ref} by selecting the optimum accessible vectors for each period in such a manner that the average of the imposed vectors should equal the V_{ref}.



(a) Short vector-100 (b) Short vector-211.

Fig. 2. depicts a schematic representation of the equivalent circuit & the current (I_c) with two distinct short vectors.

Eqn. (1) elucidates the statistical correlation amongst the timing of the imposed vectors & the timeline of the V_{ref}.

$$T_s\vec{\vec{V}}_{ref} = \sum_{i=1}^{n} T_i\vec{V}_i \quad (1)$$

$$T_s = \sum_{i=1}^{n} T_i$$

The parameter Ts in Eqn. (1) represents the time span, which ideally should be minimized. This duration can be considered as the control upgrade time span during which a mean vector is calculated. T_i denotes the time segment corresponding to a selected inverter vector, & n represents the number of vectors utilized.

In a broader context, when the reference set comprises 3 distinct vectors (n = 3), Eqn. (1) can be transformed into 3 distinct equations with 3 independent variables to be estimated (T_1, T_2, & T_3). Many vectors PWM systems, as referenced in [6–7], [9–11], & [13–15], utilize a similar timing validity & reliability approach.

Fig. 1 (b) illustrates the space vector schematic of a 3-level inverter designed for balanced dc-link capacitors [6]. This schematic offers 27 switching states, allowing for the selection of one of 19 different voltage vectors. The diagram demonstrates the distribution of counts among each vector, representing the switching signals of the inverter phases. These voltage vectors are categorized into five main groups based on their magnitude & their impact on various V_c values from the inverter AC mains. These groups consist of 6 long vectors (200, 220, 020, 022, 002, & 202), 3 zero vectors (000, 111, & 222), 6 moderate vectors (210, 120, 021, 012, 102, & 201), 6 upper short vectors (211, 221, 121, 122, 112, & 212), & 6 lower short vectors (211, 221, 121, 122, 112, as well as 212), along with (100, 110, 010, 011, 001, & 101).

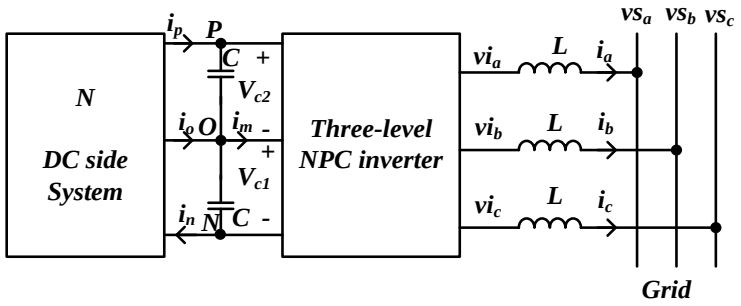


Fig. 3. Grid-connected 3-wire 3-level inverter.

If one vector ($\vec{V}_i$) is short, two alternatives will have the same impact on the AC side of the inverter in a 3-wire connection (assuming balanced voltages). On the AC side of the inverter, "211" has the same effect as "100." However, this option would require an alternate DC capacitor for power transmission to or from the AC side, which would affect the DC side.

Consequently, various capacitors would be charged / discharged based on the switching states & the direction of the AC-side current. Fig. 2 illustrates the capacitor connections if "100" or "211" is selected, highlighting the unique capacitors involved in power transfer.

Capacitor balancing has been a standard practice in most recognized 3-level NPC inverter implementations, alongside the careful selection of short vectors. The vector schematic in Fig. 1(b) serves as the basis for generating the AC-side waveform, assuming the DC voltage (V_C) is balanced. Subsequently, Fig. 1(b) is utilized to identify suitable vectors & their respective timeframes (T_i) for implementing the correct V_{ref} based on the Eqn. (1). While the control network endeavors to maintain balanced V_C, any transient imbalance or unforeseen event can lead to an erroneous AC-side waveform diverging from the control network's desired vector. This deviation might result in the generation of even harmonics, unbalanced currents, & unexpected dynamic behavior.

However, in certain scenarios, the requirement for balanced V_C may be overly restrictive. V_C can exist in either balanced or unbalanced states. The presented modification suggests that the ability to produce an correct reference vector based given in Eqn. (1) is crucial in such applications, regardless of $V_{C's}$ balance status, to achieve the system's objectives.

C. Unbalanced Vcs

Fig. 3 depicts the overall architecture of a grid-connected 3-level inverter, including both the DC & AC terminals. In particular applications of the inverter, the DC-side configuration, designated as "N," may include multiple circuit topologies. This may encompass a solar photovoltaic system, a wind generator equipped with a rectifier circuit, a battery, or a combination of these components, each exhibiting unique or identical Vdc across the capacitors.

The main objective of this article is to present an overview of the switching effects associated with a 3-wire connection of a 3-level NPC inverter, particularly when integrated with various applications on the DC side. In a 3-wire configuration of a 2-level inverter, the dq0 field, V_d, V_q, & V_0 of the inverter in vector control demonstrate two distinct operational modes within the control scheme. The zero-sequence voltage, V_0, does not influence the operational characteristics of the network on either the DC/ AC sides of the inverter.

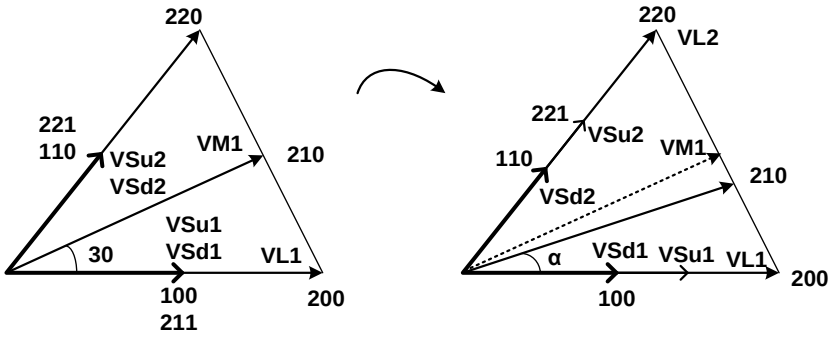


Fig. 4. Vector illustration in its first sector of Fig.1 (b) demonstrating the transformation of vectors have used stable DC & unstable DC while presuming V_{c1} V^{c2}.

Additionally, in the 3-level 3-wire configuration illustrated in Fig. 3, with constant V_d & V_q, the V0 inverter operates effectively in both stable & unstable V_c conditions, consistently generating the required voltages on the ac side. One technique involves effectively combining two solar modules with various MPPT coordinates. This

includes connecting a PV module across two capacitors, along with integrating batteries between the capacitors, or linking battery storage to each capacitor to facilitate the transfer of multiple outputs from each battery network.

D. Unbalanced Vc's *Impact on the Vector Diagram*

In instances where the V_c capacitors exhibit an imbalance, the amplitudes & angles of the short & medium vectors diverge from those associated with the balanced V_c, as demonstrated in the vector diagram presented in Fig. 1(b). Fig. 4 illustrates the differences among the various notations in the initial sector of the sextant as depicted in Fig. 1(b) when V_{C1} is less than V_{C2}.

The subsequent vector can sometimes be determined based on the switching state $\vec{V}_I$ [20].

$$\vec{V}_I = \frac{2}{3}(V_{aN} + \vec{a}V_{bN} + \overrightarrow{a^2}V_{cN}) \tag{2}$$

Where, $\vec{a} = e^{j(2\pi/3)}$ & V_{aN},V_{bN} & V_{cN} are indeed the voltages of each phase with reference to "N" in that Fig. Assuming that the length of the long vectors ((2/3)V_{dc}) is 1 unit & the voltage of capacitor C_1 ,V_{c1}= hV_{dc}, for $0 \le h \le 1$, then the vectors in the 1st sector could be figure out as per Eqn. (2) & the outcomes are shown in Eqn. (3)-(9)

$$\vec{V}sd1 = h \tag{3}$$

$$\vec{V}su1 = 1 - h \tag{4}$$

$$\vec{V}l1 = 1 \tag{5}$$

$$\vec{V}l2 = \frac{1}{2} + \frac{\sqrt{3}}{2}j \tag{6}$$

$$\vec{V}sd2 = h\left(\frac{1}{2} + \frac{\sqrt{3}}{2}j\right) \tag{7}$$

$$\vec{V}su2 = (1 - h)\left(\frac{1}{2} + \frac{\sqrt{3}}{2}j\right) \tag{8}$$

$$\vec{V}m1 = \left(1 - \frac{h}{2}\right) + h\frac{\sqrt{3}}{2}j \tag{9}$$

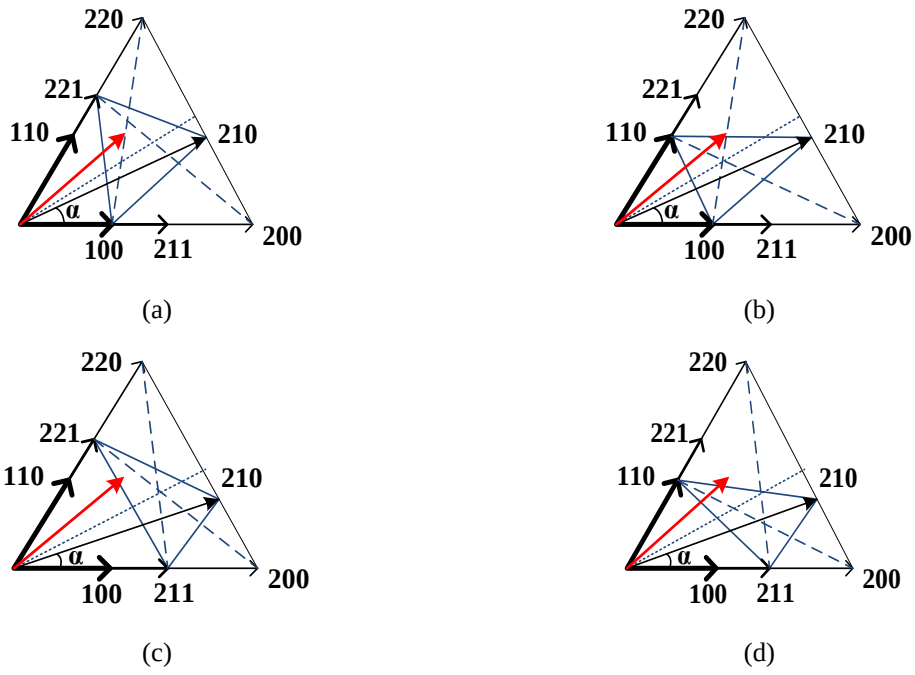


Fig. 5. Various vector shortlisting concepts.

The vectors in other sectors could be computed in the same way. As shown by Eqn. (3)-(9), the amplitudes, as well as angles of the vectors, could indeed change up to the value of the V_c. For e.g., once h = 0.5, the two V_c are about the same $\vec{V}_{sl1} = \vec{V}_{su1}$, & so are the two short vectors, Whenever the two V_c become distinct, the amplitudes of the vectors would be distinct. Because the amplitudes of short vectors have indeed changed, the choice of such short vectors would then have a significant effect on both the DC & AC sides.

Typically, for every couple of short vectors, it has been assumed redundant, because selecting any one of the short vectors at any time has the same impact on the AC end. Nevertheless, whenever the two V_c differ, the short vectors are no longer considered redundant. As a result, if $h \neq 0.5$ each short vector needs a separate timing to produce the demanded vector based on Eqn. (1).

E. Vector Selection under Unbalanced Vdc Situations & About their Consequences on the Inverter's Ac Supply

Possible combinations could be used to produce a reference vector focused on (1). Fig. 5 depicts various vector choices that could be used to produce a reference vector ($\vec{V}^*$) in the first sector based on the choice of various short vectors. For eg, to produce $\vec{V}^*$ premised on Fig. 5 (a), one of the following states with correct timing could be chosen: (1). The possible combinations are as follows: (221–210–100), (221–220–100), (000–220–Zero), (220–200–Zero), where "zero" can be "000," "111," or "222."This illustrates that there is some leeway in selecting the appropriate vector choices. Even though each of these choices can start generating a same reference vector, their own immediate effects on the DC & AC sides of the inverter are different. The correctness of the generated voltage must all be analyzed in order to evaluate the ac-side behavior.

In terms of the ac side, the demanded voltage $\vec{V}^*(t)$ should ideally be generated exactly & simultaneously in the 3 phases of the inverter in order to have the correct instantaneous current on the ac side of the system. However, due to the inverter's inability to generate the exact value of the requested voltage $\vec{V}^*(t)$ in each phase, only the average value of the demand vector for the stipulated time period of T_s could be generated in the short time T_s.

An error vector $\vec{e}(t)$ could be evaluated to find how far the generated voltage detracts from the demanded vector in order to assess the continuous-time behavior of the ac-side voltages as described in the following:

$$\vec{e}(t) = \overrightarrow{V^*}(t) - \overrightarrow{V_{apl}}(t) \tag{10}$$

$$E(t) \triangleq \left| \int_0^t \vec{e}(t)dt \right|; \ 0 \leq t \leq T_s \tag{11}$$

Where $\vec{V}_{apl}(t)$ is the applied vector at the time "t". This error can result in harmonic current across the impedance connected between the inverter & the grid. If this impedance is an inductor, then the ripple in the inductors current $\vec{I}_{rL}$ can be expressed as

$$\vec{I}r_L = 1/L \int_o^t \vec{e}(t)dt \tag{12}$$

where $\vec{e}(t)$) is defined as

$$\vec{e}(t) \triangleq L \frac{d\vec{I}r_L}{dt} \tag{13}$$

To obtain Eqn. (13), it must be presumed that the demanded vector $\vec{V}^*(t)$ will now produce sinusoidal current as in an inductor, which is usually appropriate in the network's continuous time behavior

F. Selecting Vectors under Unbalanced Vdc

Throughout aspects of a DC side, distinct vectors have various impacts on the V_c, that are determined by the total amount of the incoming currents from the DC as well as inverter sides.

Fig. 3 depicts the DC-side network currents i_p, i_o, & in, that are affected by the DC-side network circuit as well as V_c. Currents flowing through the inverter's switches as well as the AC side of an inverter could be significantly impacted by vector that also are performed by the inverter. Distinct vectors would then transfer alternating current as well as power to capacitors in various ways, as noted previously. Instantaneous power transmitted from the AC side to the DC side of the inverter could be calculated using the following equation:

$$p(t) = v_{Ia}.i_a + v_{Ib}.i_b + v_{Ic}.i_c \tag{14}$$

in which ac-side instantaneous voltages vIa, vIb, & vIc were referenced to the "N" point as well as ac-side instantaneous currents ia, ib, ic were inverters currents.

Again, for short vector, for instance, the model equation could be used to describe p(t) in the 1st sector of the vector shown in Fig. 4:

$$p211(t) = (1-h)Vdci_a \tag{15}$$

$$p100(t) = hVdc * (-i_a)$$

$$p221(t) = (1-h)Vdc * (-i_{c)} \tag{16}$$

$$p110(t) = hVdc * i_c$$

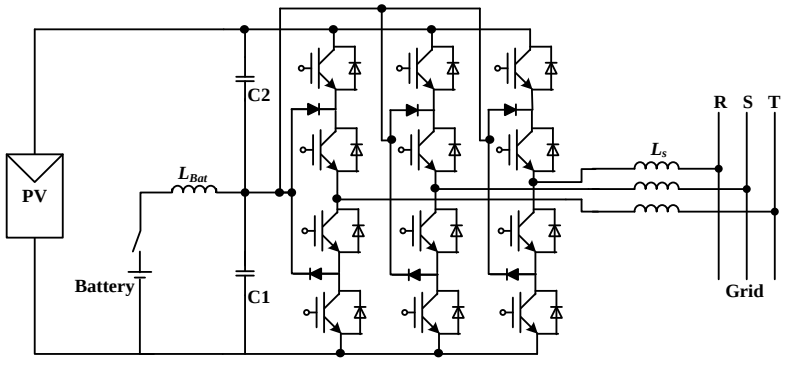
Neglecting the dc-side control flow, choosing the upper short vectors "211" & "221," affects the upper V_c, as well as choosing the lower short vectors, "100" & "110," affects the lower V_c. Once ia > 0, for instance, if vector "211" has been chosen, this would begin charging the upper capacitor without affecting the lower V_c, whereas vector 100 would then eject the lower capacitor without affecting the upper V_c.

III.ENVISAGED TOPOLOGY FOR EMBEDDING PV - BATTERY STORAGE, AS WELL AS GOVERN

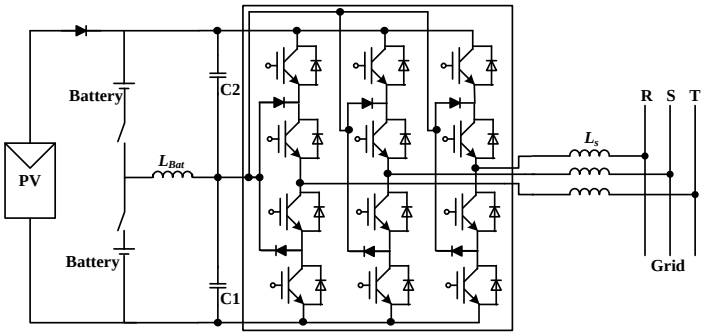
A. Envisaged Topology for Integrating Photovoltaic PV - Battery Storage Using a 3-Level Inverter's Enhanced Imbalance DC Capabilities

Based on the past section's discussions, Fig. 6 presents 2 additional provisions of a 3-level inverter to integrate battery bank as well as solar PV, in which neither supplementary multilevel inverter has been needed to interact the energy storage to a wire PV network. These could assist in enhancing the overall performance of the system, especially in middle-to-high power application areas.

The general structure is depicted in Fig. 6 (a). Power from the RES can indeed be converted to grid power in the present scheme, whereas the control scheme can charge & discharge the battery as needed.



(a) The fundamental arrangement;



(b) Improved arrangement.

Fig. 6. Incorporating solar PV & battery

The presented network will assist in regulating the total amount of V_c, while this arrangement may work in most cases, when the PV does not generate any output, the network cannot function properly with only one battery.

Fig. 6(b) exhibits better structure, which connects two batteries via two relay nodes via two capacitors once more. Because one of the relay nodes has been turned off & the other has been turned on, the structure in Fig. 6(b) would be equivalent to something in Fig. 6(a), where the battery could be charged or discharged & the RES can produce power. When it appears that RE is not existent, every one of these relays could be shut, enabling the DC bus to transmit or absorb P & Q from as well as from the grid. It should have been mentioned that such relays have been set to be ON or OFF even though requested, with no need for PWM control. Then, at first when energy has been provided from the RES or the grid, it allows for greater control over which of the two batteries has been charged. If one of the batteries has been charged, the relay associated with it can be set to open while the relay associated with the other battery is set to close to charge.

To ensure uninterrupted inductor current as well as preventing damage to the relay, caution must be taken to help ensure that the current flowing L_{batt} is zero associated with opening any of these relays.

Control Architectures

Fig. 6(b) illustrates 3 potential relay configurations: 1) the upper relay in a closed state, 2) the bottom relay in a closed state, & 3) both relays in a closed state. Fig. 7 illustrates the graphical representation of the control network for Arrangement 1. The supervisory block of the network will subsequently assess the requirements for P & Q power generation by the inverter intended for transmission to the grid, as illustrated in Fig. 7. The accomplishment of this task will utilize the existing photovoltaic generation, grid data, & specifications of the battery pack.

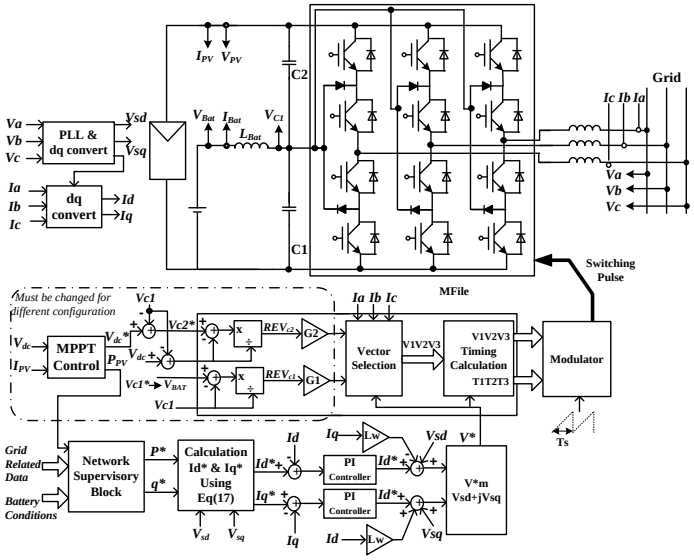


Fig. 7. A proposed PV-energy storage integration control

To accomplish the MPPT circumstance, the MPPT component determines the appropriate V_{dc} across the PV. This output can be calculated by employing a slower-dynamic control loop & measuring the obtainable PV power. The MPPT controller used to obtain the required V*dc is fully explained in [3-4].

As used in Eqn. (17), the requested inverter current in the d_q-axis, i_d, & i_q could be evaluated by the demanded P & Q as well as the V_{grid} in the dq-axis, V_{sd}, & V_{sq}.

The inverter's demanded voltage vector can be determined using a PI controller & a decoupling control method. Fig. 7 shows the conceptual control scheme. To transfer a set quantity of power to the grid, the new method calls for charging the battery with excess PV power or discharging it to help the PV power when the latter is unable to meet the demand.

A correct sector in a vector diagram can all be calculated upon analyzing the demanded V_{ref} vector.

The relative errors of V_c provided in (18) & (19) have been used to evaluate which of the short vectors should be chosen.

$$e_{Vc1} = \frac{V_{C1}^{*} - V_{C1}}{V_{C1}} \tag{18}$$

$$e_{Vc2} = \frac{V_{C2}^{*} - V_{C2}}{V_{C2}} \tag{19}$$

Under which V_{C1} & V_{C2} are the desired & actual V_c for capacitors C_1 & C_2, in both.

The choice of the short vectors determines whether the capacitor would be to be charged or discharged. The short vector should always be picked depends on the error levels of the capacitor voltages and how effective they are on the behavior of the control circuit.

Predicated here on the concept, a judgment process "F," as shown in (20), could be described.

$$F = G_1 e_{Vc1} - G_1 e_{Vc2} \tag{20}$$

Where G_1 & G_2 represent the gains related to the V_c relative errors.

IV.THE ENVISAGED CONFIGURATION AS WELL AS CONTROL NETWORK'S COMPUTATION AND VERIFICATION

To validate the efficacy of the suggested configuration as well as system design, simulations were done in MATLAB. To interact inverter to the grid, an LCL filter has been used. Fig. 8 depicts the designed to simulate system's graphical representation. In the simulated in MATLAB software, 3 series-connected PV modules have been used in Eqn. (21) [21] provides the statistical model for each of the PV units, that are used in the computation

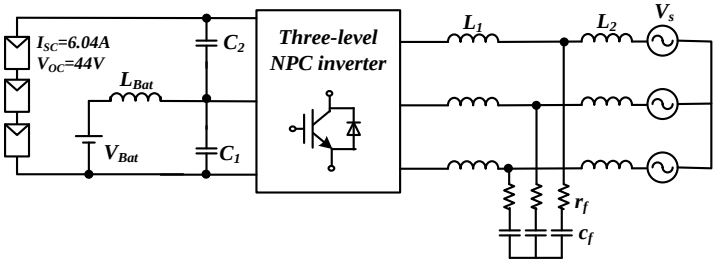


Fig. 8. Flowchart of modeled infrastructure.

Table 1. modeled infrastructure simulation variables

V_{BAT}	Vs(line)	L_{BAT}	C_1,C_2	L_l	L_s
60 V	50 V	5 mH	1000 µf	500 µH	900 µH
r_f	C_f	K_p	K_i	G_1	G_2
3Ω	14µf	2.9	1700	1	200

$$I_{PV} = I_{SC} - 10^{-7}\left(e^{\left(\frac{V_{PV}}{2574\times10^{-3}}\right)} - 1\right) \quad (21)$$

At which point, I_{SC} is indeed the PV's short circuit current.

As in computation, it is therefore supposed that I_{SC} varies with irradiance. With a solar irradiation of 1000 W/m^2, I_{SC} equals 6.04 amperes as well as the PV panels' Voc equals 44 V. The table illustrates the basic specifications of the simulation environment. As can be seen in Table 1, one such value was chosen to be 200 in order to obtain better control over V_{dc}.

The purpose of an L_{BAT} would be to smooth the I_{bat}, particularly in transient conditions. For the inductor value, a wide range of values is appropriate; even so, reducing its value will boost the I_{bat} overshoot. Its valuation is also affected by the value of the adjacent capacitor & the transient voltages. Due to considerations of practicality a low value for LBAT has been selected, with 5 mH being chosen based on simulated outcomes.

Building a model in the framework in the dq-frame yields values of K_p & K_i. Using the decoupling methodology seen in Fig. 7, the current control loop could be transformed into a simplified situation [22] contains more information on this method.

Two different cases were designed to simulate these conceptual objectives to explore the efficacy of the suggested configuration as well as control techniques to use a step-change in the reference inputs underneath the below:

- The effect of a step-change in the amount of P & Q requested to be transmitted to a grid, assuming constant solar irradiance.
- The same effect as a step change in solar irradiation when the grid's demanded P & Q remain constant.

A. Case 1:

It is assumed that under case 1, solar irradiation will cause the PV panel to produce I_{SC} = 5.61 A. In order to achieve Pmax from of the PV architecture, which becomes capable of producing 558 W of power generation (as shown in Fig. 7), this same MPPT determines the required voltage V_{dc} of 117.3 V for the PV panels.

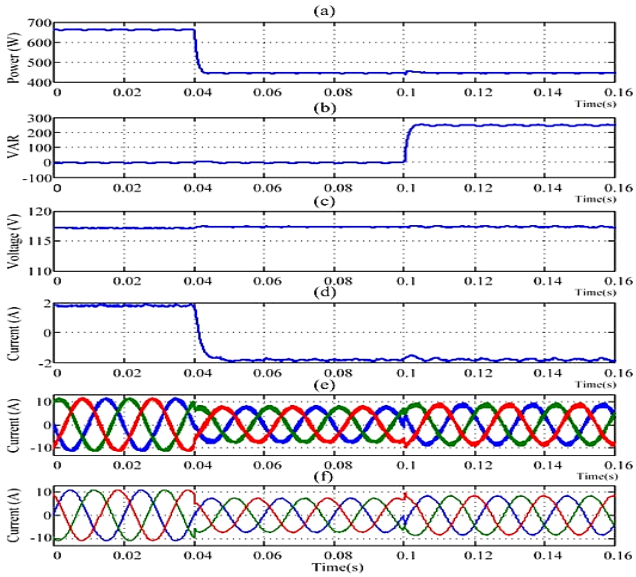


Fig. 9. Simulated outcome for the case 1 (a) P_{inj} to the grid. (b) Q_{inj} to the grid.

(c) PV module Vdc I_{bat}. (e) Inverter AC current. (f) Grid current.

At time step t = 40 ms, the Q changes from 0 to 250 VAr, while the needed P to the grid, which was initially set at 662 W, afterwards drops to 445 W. The results of this calculations are shown in Fig. 9. Fig. 9(a) & (b) display the successful implementation of the requisite P & Q by the suggested control algorithm, & Fig. 9(c) demonstrates a accurate regulation of a PV voltage (to be 177.3 V) to extract the maximum power from the PV module. Battery drains when grid power is higher than PV power, & charges when PV power is higher than grid power, as present

in Fig. 9(d). As can be seen in Fig. 9(d), the PV output is insufficient to prevent the battery from discharging at 1.8 A before time t = 40 ms. When the I_{bat} drops to around -1.8 A after t = 40 ms, the battery was being charged by PV component's overflow power. Grid-side currents with a THD lesser than 1.29 % due to the LCL filter is shown in Fig. 9(f), whereas inverter ac-side currents depicted in Fig. 9(e). Results, depicted in Fig. 9, show that the entire system has excellent dynamic characteristics.

The inverter waveforms for about the same case are shown in Fig. 10. Fig. 10 (a) depicts the V_{ab}, while Fig. 10 (b) depicts the inverter's phase-to-midpoint voltage V_{ao}. Fig.s 10(c) & (e) shows V_{ao}, V_{on}, & V_{an} after numerical filtration to determine the average value of the PWM waveforms.

B. Case 2:

In Case 2, it is assumed that the solar radiation intensity varies, leading the PV module to generate ISC values of 4.8, 4, & 5.61 A. To optimize power extraction from the PV units, the MPPT control algorithm calculates that V_{dc} should be set to 115.6, 114.1, & 117.3 V, respectively, resulting in power outputs of 485, 404, & 558 W.

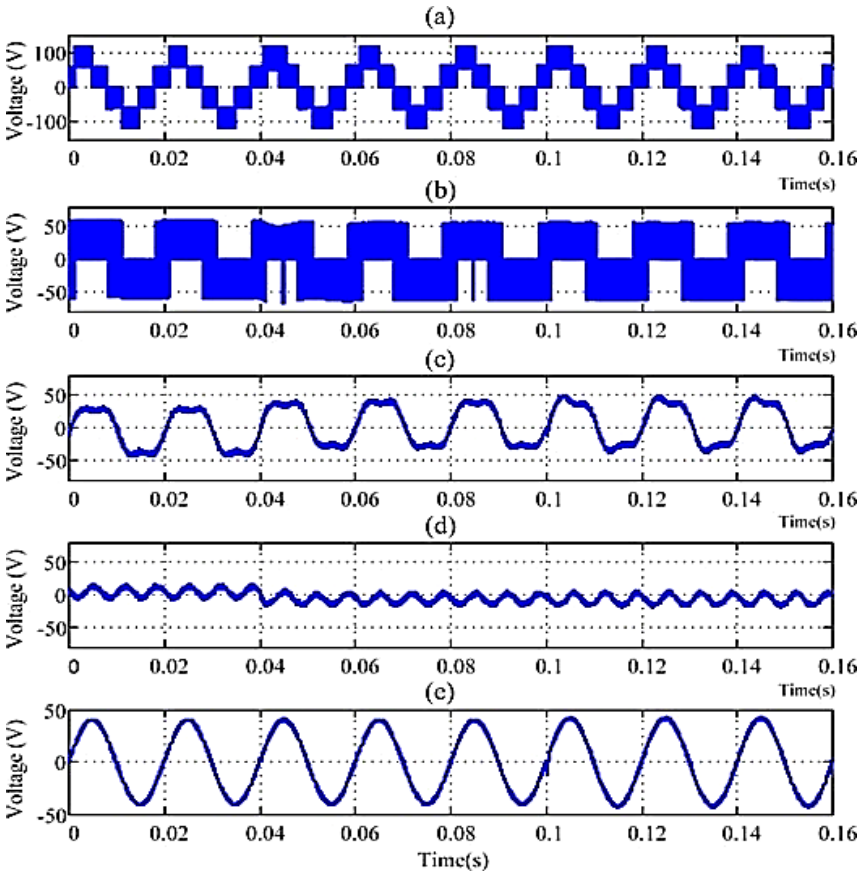


Fig. 10. Output waveform generated by a modeled inverter. a) V_{ab}, or the voltage at the inverter. b) The voltage reference for the Centre of the V_{ao}-phase. Inverter's (c) Von-filtered midway voltage reference for inverter phases. Reference voltage set at DC filtered von-filtered neutral. Voltage regulator to neutral from a filtered V_{an}-filtered phase.

Throughout the simulation, the grid demand for power (P) remains constant at 480 W, while Q is set to 0.

Fig. 11 illustrates the outputs of the Case 2 simulation. Fig. 11(a) depicts that the inverter successfully delivers the desired power output. Fig. 11(b) demonstrates the PV voltage variations corresponding to different solar irradiation levels, ensuring the PV modules produce the desired power. Fig. 11(c) indicates the proper charging & discharging of the battery, which supplements the PV power generation to meet the grid's demands. Fig. 11(d) displays the grid-side current waveform, demonstrating that the proposed PWM technique generates appropriate vectors. Notably, the inverter exhibits rapid transient response using this methodological approach. Finally, Fig. 11(e) illustrates the grid's current (I_{ph}) & voltage (V_{ph}), both maintaining acceptable levels, ensuring that Q remains at 0 throughout.

C. Application-Oriented Framework

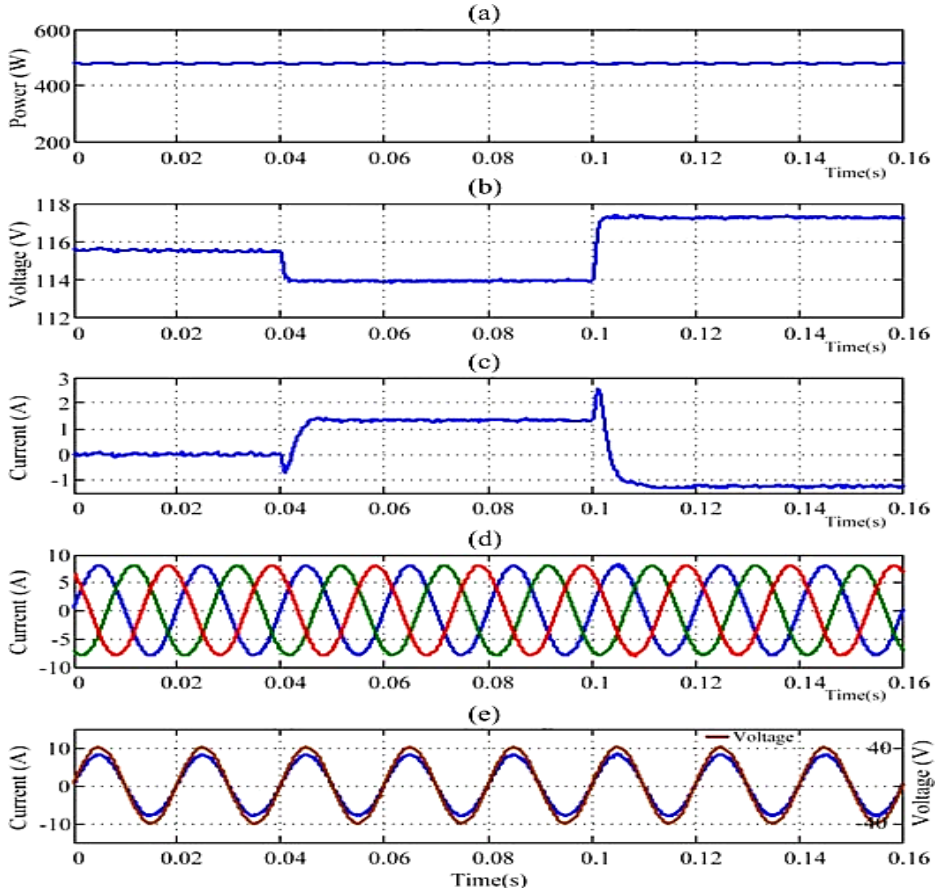
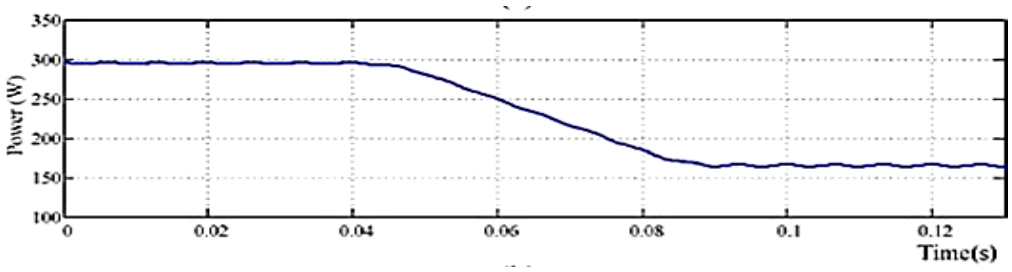


Fig. 11. The 2nd case's simulated outcomes. (a) P_{inj} to the grid. (b) PV module V_{dc}. (c) I_{bat}. (d) Grid side currents. Grid side Phase (a) voltage & it's current.

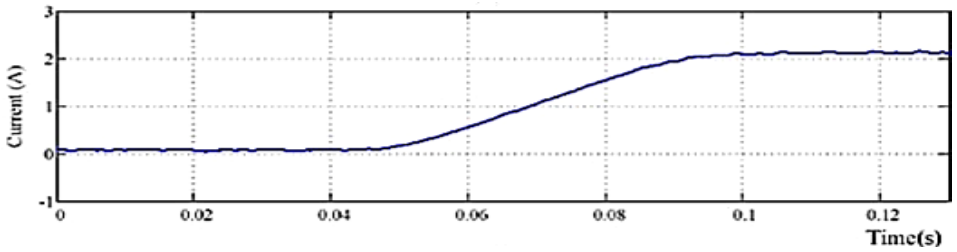
In the case 3, the target power (P) to be fed into the grid is initially set at 295 W, & at t = 40 ms, it commences a controlled decrease, stabilizing at 165 W by t = 90 ms. This implies that the solar irradiation would result in a PV module generating I_{SC} = 2.89 A [21]. To achieve MPPT the desired PV voltage i.e. V_{dc} would be set at 112.8 V to produce 305 W.

Fig. 12(a) illustrates the gradual decrease in the power transmitted to the grid, aligning with the demanded power profile. In Fig. 12(b), the I_{bat} remains approximately 0.1 A until t = 40 ms, after which it increases to around 2.2 A due to the reduced power transmission to the grid while maintaining a constant PV output. Fig. 12(c) depicts the AC inverter currents gradually decreasing from I_{rms} 3.4 at t = 40 ms to I_{rms} 1.9 at t = 90 ms.

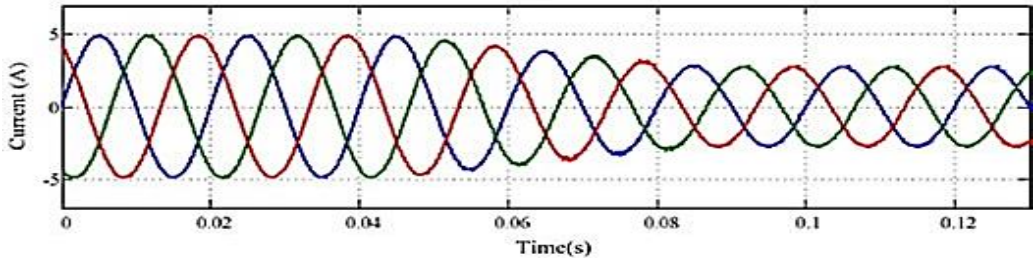
To maintain MPPT operation, the V_{dc} is managed to remain at 112.8 V throughout the simulation. It's noteworthy that the DC bus operates in an imbalanced state during the simulation, as the V_{bat} is fixed at 60 V, preventing it from equating to V_c.



(a) P_{inj} to grid



(b) I_{bat}.



(c) I_{Grid}.

Fig. 12. The outcomes of computation for third case

V.CONCLUSION

This study presents a new configuration for a 3-level Neutral Point Clamped Voltage Source Inverter (NPC-VSI) aimed at facilitating the seamless integration of RE sources & battery storage within the inverter's DC link. An innovative extended unbalanced 3-level vector modulation scheme is introduced to guarantee precise AC voltage generation, even in the presence of unbalanced DC-link voltage conditions. An advanced control algorithm has been developed to efficiently manage power flow between solar PV, battery storage, & the grid, while ensuring MPPT functionality for the PV systems is maintained.

The proposed system & control algorithm underwent comprehensive evaluation via simulations, showcasing their efficacy in regulating AC-side currents & overseeing battery charging & discharging under different solar irradiation conditions. The results confirm the robustness & efficiency of the recommended configuration, emphasizing its potential to improve the performance & reliability of hybrid energy systems. This document establishes a basis for subsequent investigations into optimizing inverter designs & control methodologies aimed at enhancing renewable energy integration & ensuring grid stability.

REFERENCES

[1] O. M. Toledo, D. O. Filho, and A. S. A. C. Diniz, “Distributed photo- voltaic generation and energy storage systems: A review,” Renewable Sustainable Energy Rev., vol. 14, no. 1, pp. 506–511, 2010.

[2] M. Bragard, N. Soltau, S. Thomas, and R. W. De Doncker, “The balance of renewable sources and user demands in grids: Power electronics for modular battery energy storage systems,” IEEE Trans. Power Electron., vol. 25, no. 12, pp. 3049–3056, Dec. 2010.

[3] A. Yazdani and P. P. Dash, “A control methodology and characterization of dynamics for a photovoltaic (PV) system interfaced with a distribution network,” IEEE Trans. Power Del., vol. 24, no. 3, pp. 1538–1551, Jul. 2009.

[4] A. Yazdani, A. R. Di Fazio, H. Ghoddami, M. Russo, M. Kazerani, J. Jatskevich, K. Strunz, S. Leva, and J. A. Martinez, “Modeling guidelines and a benchmark for power system simulation studies of 3-phase single-stage photovoltaic systems,” IEEE Trans. Power Del., vol. 26, no. 2, pp. 1247–1264, Apr. 2011.

[5] M. A. Abdullah, A. H. M. Yatim, C. W. Tan, and R. Saidur, “A review of maximum power point tracking algorithms for wind energy systems,” Renewable Sustainable Energy Rev., vol. 16, no. 5, pp. 3220–3227, Jun. 2012.

[6] Burusteta, J. Pou, S. Ceballos, I. Marino, and J. A. Alzola, “Capaci- tor voltage balance limits in a multilevel-

converter-based energy storage system," in Proc. 14th Eur. Conf. Power Electron. Appl., Aug./Sep. 2011, pp. 1–9.

[7] L. Xinchun, Shan Gao, J. Li, H. Lei, and Y. Kang, "A new control strategy to balance neutral-point voltage in 3-level NPC inverter," in Proc. IEEE 8th Int. Conf. Power Electron. ECCE Asia, May/Jun. 2011, pp. 2593–2597.

[8] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[9] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space-vector pulsewidth modulation for 3-level npc converter with the neutral point voltage control," IEEE Trans. Ind. Electron., vol. 58, no. 11, pp. 5076–5086, Nov. 2011.

[10] J. Pou, D. Boroyevich, and R. Pindado, "Effects of imbalances and non-linear loads on the voltage balance of a neutral-point-clamped inverter," IEEE Trans. Power Electron., vol. 20, no. 1, pp. 123–131, Jan. 2005.

[11] Z. Huibin, S. Jon Finney, A. Massoud, and B. W. Williams, "An SVM algorithm to balance the capacitor voltages of the 3-level npc active power filter," IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2694–2702, Nov. 2008.

[12] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Cor- balan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 305–314, Feb. 2009.

[13] W. Chenchen and L. Yongdong, "Analysis and calculation of zero- sequence voltage considering neutral-point potential balancing in 3- level npc converters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2262–2271, Jul. 2010.

[14] S. Busquets-Monge, S. Somavilla, J. Bordonau, and D. Boroyevich, "Ca- pacitor voltage balance for the neutral-point-clamped converter using the virtual space vector concept with optimized spectral performance," IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1128–1135, Jul. 2007.

[15] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest 3 virtual space vector PWM—A modulation for the compre- hensive neutral-point balancing in the 3-level NPC inverter," IEEE Power Electron. Lett., vol. 2, no. 1, pp. 11–15, Mar. 2004.

[16] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a 3-level neutral-point-clamped converter," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 642–651, Feb. 2012.

[17] J. Wei-dong, D. Shao-wu, C. Liu-chen, Y. Zhang, and Q. Zhao, "Hybrid PWM strategy of SVPWM and VSVPWM for NPC 3-level voltage- source inverter," IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2607–2619, Oct. 2010.

[18] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibaez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutral- point-clamped converter," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 294–304, Feb. 2009.

[19] Z. Jian-Yong, S. Zhang-Liang, M. Jun, and L.-f. Wang, "An improved neutral-point voltage balancing algorithm for the npc 3-level inverter based on virtual space vector PWM," in Proc. Int. Conf. Elect. Control Eng., Jun. 2010, pp. 3283–3287.

[20] J. Pou, D. Boroyevich, and R. Pindado, "New feedforward space-vector PWM method to obtain balanced AC output voltages in a 3-level neutral-point-clamped converter," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1026–1034, Oct. 2002.

[21] M. G. Villalva, J. R. Gazoli, and E. R. Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays," IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1198–1208, May 2009.

[22] A. Yazdani and R. Iravani, Voltage-Sourced Converters in Power Systems. New York, NY, USA: Wiley,

2010.

[23] S. S. Hakami and K. -B. Lee, "Enhanced Predictive Torque Control for 3-Level NPC Inverter-Fed PMSM Drives Based on Optimal Voltage Magnitude Control Method," in IEEE Transactions on Power Electronics, vol. 38, no. 3, pp. 3725-3738, March 2023, doi: 10.1109/TPEL.2022.3226720.

[24] S. M. Mozayan, M. Saad, H. Vahedi, H. Fortin-Blanchette and M. Soltani, "Sliding Mode Control of PMSG Wind Turbine Based on Enhanced Exponential Reaching Law," in IEEE Transactions on Industrial Electronics, vol. 63, no. 10, pp. 6148-6159, Oct. 2016, doi: 10.1109/TIE.2016.2570718.

[25] F. Guo, T. Yang, A. M. Diab, S. S. Yeoh, S. Bozhko and P. Wheeler, "An Enhanced Virtual Space Vector Modulation Scheme of 3-Level NPC Converters for More-Electric-Aircraft Applications," in IEEE Transactions on Industry Applications, vol. 57, no. 5, pp. 5239-5251, Sept.-Oct. 2021, doi: 10.1109/TIA.2021.3085798.

[26] N. Khosravi, S. Echalih, Z. Hekss, R. Baghbanzadeh, M. Messaoudi and M. Shahideipour, "A New Approach to Enhance the Operation of M-UPQC Proportional-Integral Multiresonant Controller Based on the Optimization Methods for a Stand-Alone AC Microgrid," in IEEE Transactions on Power Electronics, vol. 38, no. 3, pp. 3765-3774, March 2023, doi: 10.1109/TPEL.2022.3217964.

[27] S. S. Hakami and K. -B. Lee, "Enhanced Predictive Torque Control for 3-Level NPC Inverter-Fed PMSM Drives Based on Optimal Voltage Magnitude Control Method," in IEEE Transactions on Power Electronics, vol. 38, no. 3, pp. 3725-3738, March 2023, doi: 10.1109/TPEL.2022.3226720.

[28] X. Cai, Z. Zhang, J. Zhang, Z. Li, R. Kennel and Z. Zhang, "Improved Predictive Control of 3-Level-NPC Power Converters," 2021 IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE), Jinan, China, 2021, pp. 393-402, doi: 10.1109/PRECEDE51386.2021.9680960.

[29] A. Tregubov, P. Karamanakos and L. Ortombina, "A Computationally Efficient Robust Direct Model Predictive Control for Medium Voltage Induction Motor Drives," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Vancouver, BC, Canada, 2021, pp. 4690-4697, doi: 10.1109/ECCE47101.2021.9595296.

[30] N. Khosravi, S. Echalih, Z. Hekss, R. Baghbanzadeh, M. Messaoudi and M. Shahideipour, "A New Approach to Enhance the Operation of M-UPQC Proportional-Integral Multiresonant Controller Based on the Optimization Methods for a Stand-Alone AC Microgrid," in IEEE Transactions on Power Electronics, vol. 38, no. 3, pp. 3765-3774, March 2023, doi: 10.1109/TPEL.2022.3217964.

[31] P. Katta, D. Joseph, M. O. A, H. S and S. P, "Power Control of Solar Grid-Tie Inverter Using Bidirectional DC-DC Converter," 2022 International Conference on Power, Energy, Control and Transmission Systems (ICPECTS), Chennai, India, 2022, pp. 1-4, doi: 10.1109/ICPECTS56089.2022.10047126.