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Comparative Study of the Total Harmonic Distortion Voltage Evaluation for a Multilevel Inverter

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Abstract: - This study presents comparison analysis between a theoretical evaluation method and analytical evaluation method of voltage Total Harmonic Distortion (THD) for single phase multilevel pulse width modulation (PWM) inverter. The first method consists of using a time domain approach which provides piecewise analytical solutions accounting for all switching harmonics. This approach is an alternative to a numerical method in the frequency domain with limited harmonics count and infinite double Fourier series expansion. The method is based on the Normalized Mean Square (NMS) criterion to calculate voltage Total Harmonic Distortion. The chosen topology for the Multi-Level Inverter (MLI) is the cascaded H-Bridge multilevel (CHB-MLI). The second method consists of measuring THD in Matlab/Simulink for an arbitrary number of inverter levels (L) but a frequently number encountered in the literature or in practice. Modulation index (m) is varied between 0.1 and 1 in small steps. The obtained results in both methods are compared and carried out in graphs for each level of the inverter.

Keywords: Multilevel inverters, Normalized Mean Square. Cascaded H-Bridge, Total harmonic distortion.

I. INTRODUCTION

One of the oldest indexed articles relating to the subject of the present article dates back to 1962. This paper [1] discusses the rapid improvement of semiconductor power devices at this time. This led, according to the author, to an accelerated introduction of new equipment for the conversion of electrical energy. The reliability and efficiency in converting direct current to alternating current has enabled the development of solid-state inverter designs for a number of applications such as emergency power supplies, frequency controlled sources and frequency converters.

In paper [2] published on 1967, the author used high-frequency pulse width modulation in a DC/AC inverter to provide low-frequency sine wave output without using a low-frequency power transformer or filter components low frequency. In addition to its physical characteristics (size and weight), the inverter was self-regulating. Analysis of its circuit and output waveform provided the mathematical basis that validated the experimental results. Paper [3] published on 1979, has presented a DC/AC converter capable of producing up to three-level voltage and including two transistorized switching amplifiers operable each to two different conditions. Authors used a control circuit for driving the transistorized switching amplifiers and providing multi-phase voltage waveforms. Already at that time, there were circuits designed for converting direct voltage into alternating voltage and for synthesizing electrical waveforms but at a fixed frequency or over a restricted frequency range. These were very complex circuits, with many of components, which reduced their reliability and increased their cost. The citation of these three articles - on a non-exhaustive basis - is a tribute to the pioneers of this branch of technology. After this time, inverters like all other devices evolved very quickly, gaining in both topology and efficiency. Some papers today propose multilevel inverters of up to 35 levels as in [4]. The integration of renewable energies such as photovoltaic into the network is without filter thanks to the considerable reduction in the THD voltage rate offered by the new multilevel inverters.

DC/AC multilevel inverters, also called multilevel converters are being widely used in several applications. Among the methods for optimizing their voltage and current, there are digital methods, which are known to be complex and time-consuming to carry out, such as Genetic Algorithm (GA) for the selective harmonic elimination (SHE) method in ref [5], or Particle Swarm Optimization (PSO) for SHE in [6].

The principle of the multilevel inverter is quite simple since its role is to synthesize a staircase wave. The more steps there are, the closer the waveform is to the sinusoidal form and the lower the harmonic rates. Thus, voltage THD for a 3-level inverter is much higher than that of a 5 or 7-level inverter for example. So, the question that may arise is: where is the limit on the number of levels? The answer lies in practice. There are non-feasibility constraints and in reference [7], the authors discuss issues of voltage unbalance, voltage clamp requirements, circuit layout, and packaging constraints.

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II. Topology Of Multilevel Inverter

Fig (1) presents the different types of MLIs. They are divided into two main categories, conventional MLIs and modified MLIs. It is from conventional topologies that it is possible to imagine and create any modified topology according to the fixed objective. In this work, it is the Cascaded H Bridge Multi level Inverter (CHBMLI) which will be the subject of the study but it is entirely possible to carry out the same work based on the Diode Clamped Multi level Inverter (DCMLI) topology or the Flying Capacitor Multi level Inverter (FCMLI) topology.

The H Bridge connected to a DC source is a full bridge inverter giving three voltage levels at its output. It can be considered as a basic unit for "building" higher level CHBMLI topologies. Thanks to the particularity that each complete bridge is connected to a separate DC source as shown inn Fig (2), it is easy to connect as many basic units in series with as many separate SC sources and obtain the number of voltage levels desired at the output of the assembly. The quality of the output voltage improves by increasing the number of basic units to be connected in series because the staircase shape is closer to the sinusoidal waveform. The total Harmonic Distortion decreases when the number of H-Bridges connected in series increases. Therefore, the size of the passive filter must also decrease and bring down the price which represents a good impact on the cost.

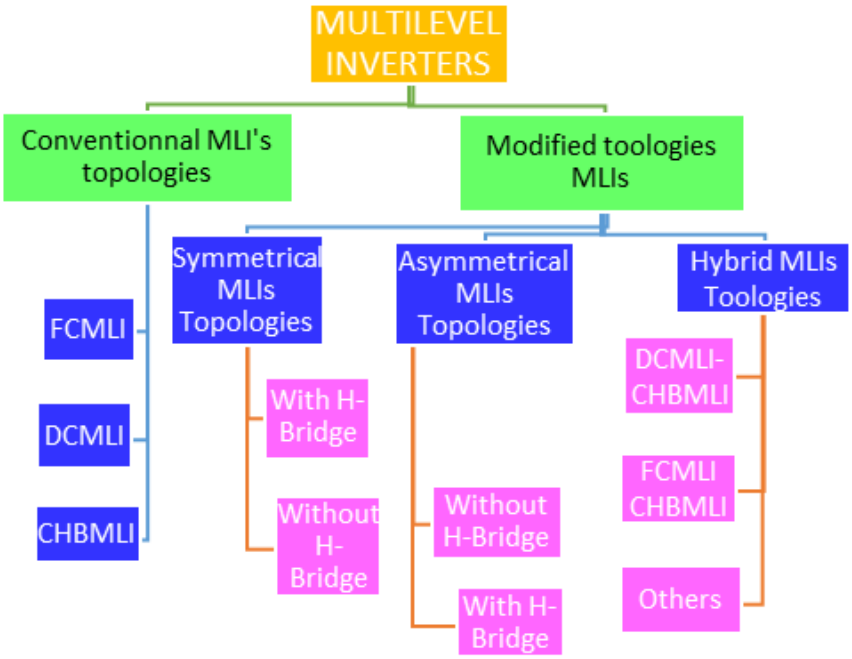

Fig. 1 Different topologies of MLIs [8]

Considering the three basic diagrams of the three topologies DCMLI, FCMLI and CHBMLI, it is obvious that CHBMLI contains fewer components than the other two topologies. This contributes firstly to facilitating assembly, avoiding clamping diodes, avoiding clamping capacitors and saving volume [14]. It should also be noted that a voltage unbalance in the intermediate circuit capacitors can cause an unbalance in the output voltage level [15].

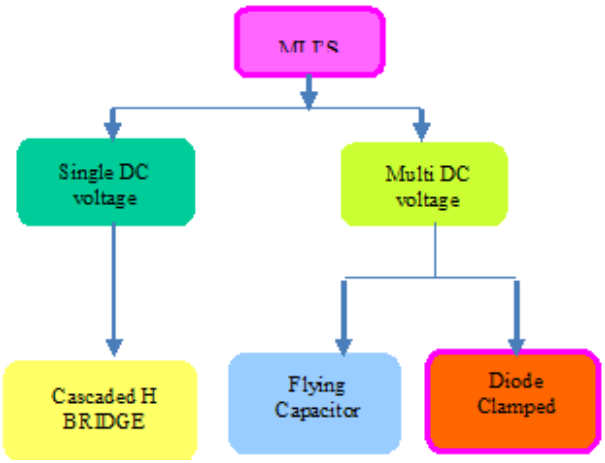

Fig. 1 Example of an unacceptable low-resolution image

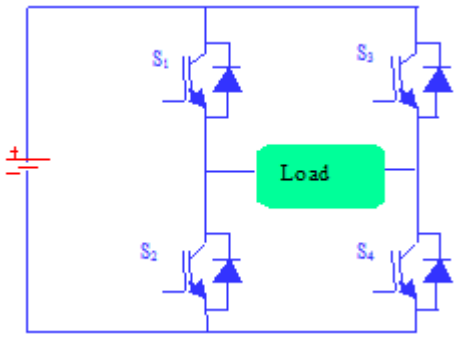

Fig.3. Three-level H-bridge MLI

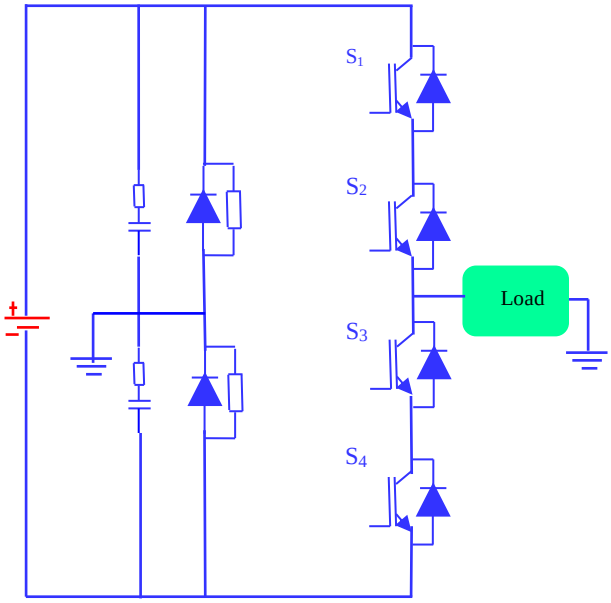

Fig. 4 Three-level diode clamped MLI

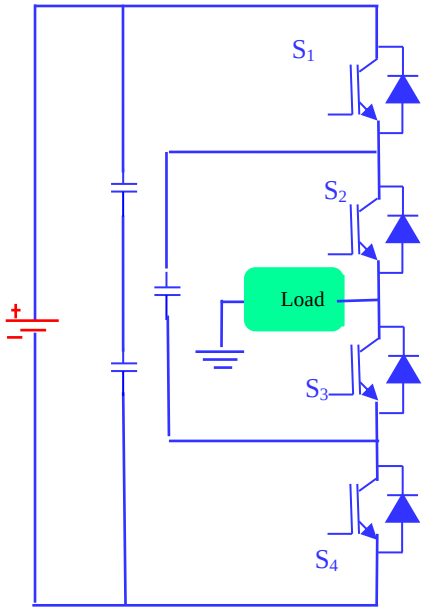

Fig. 5 Three-level Flying Capacitor MLI

III. THEORETICAL CALCULATION OF THD (%)

To avoid the problem of complex expressions of the frequency domain approach, it is possible to use the time domain approach to evaluate the power quality [8]. To go from frequency domain to time domain, it is necessary to recall the equation that links energy in the time and in the frequency domain and witch is known as the Parseval's theorem. For the periodical signal, Parseval's theorem states that the energy in one period of the signal is equal to the energy power in the spectrum [9] [10].

$$P = \frac{1}{T}\int_0^T x(t)^2 dt = \sum_{h=-\infty}^{+\infty} \left|\underline{X_h}\right|^2 \quad (1)$$

In time domain, MLI voltage quality can be evaluated by using the ripple voltage Normalized Mean Square (NMS). The NMS is defined as quadratic RMS value of the ripple voltage [11]

$$NMS = \frac{1}{T}\int_0^T u_R^2(\omega t) d\omega t \quad (2)$$

u_R: The ripple voltage, it is given as the difference of the signal voltage and the fundamental related on DC voltage by the equation [11]:

$$u_R = \frac{u(\omega t) - u_1(\omega t)}{U_{DC}} \quad (3)$$

The ripple voltage Normalized Mean Square (NMS) for H-Bridge DC PWM is given in [12] and [13] for an arbitrary number of levels L by the formula:

$$NMS_L^{DC}(D) = \left(D - \frac{i}{L-1}\right)\left(\frac{i+1}{L-1} - D\right) \quad (4)$$

D is a normalized DC voltage command. D must satisfy the following conditions according to *i* because NMS is piece-wise analytical:

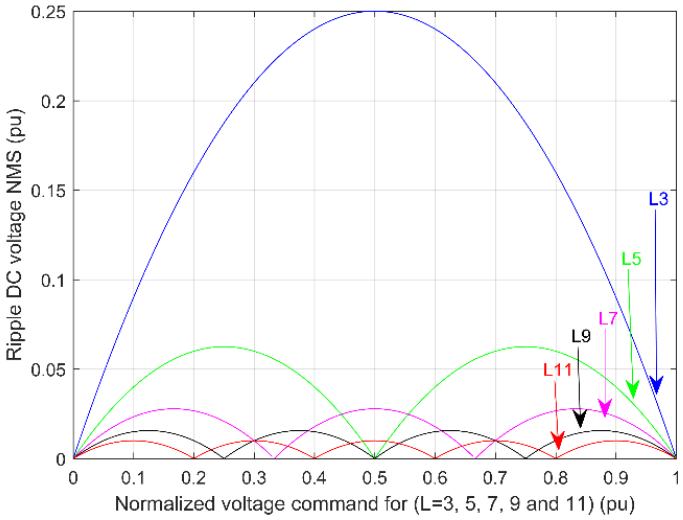

Fig. 6. NMS for H-Bridge DC PWM

Fig 6 shows NMS criterion for H-Bridge DC PWM for the most frequent numbers of levels: 3, 5, 7, 9 and 11.

The ripple voltage Normalized Mean Square (NMS) for H-Bridge AC PWM is given in [12], [13] and [14] as followed:

$$NMS_L^{AC}(m) = \begin{cases} -\frac{1}{2}m^2 + \frac{2}{\pi(L-1)}m \; 0 \le m < \frac{1}{L-1}; \\ \frac{2}{\pi(L-1)}m - \frac{1}{2}m^2 - \frac{k(k+1)}{(L-1)^2} + \frac{4}{\pi(L-1)^2}\sum_{i=1}^{k} i.\,arcsin\left[\frac{i}{(L-1)m}\right] + \\ \frac{4}{\pi(L-1)}\sum_{i=1}^{k}\sqrt{m^2 - \frac{i^2}{(L-1)^2}} \qquad \frac{k}{L-1} \le m < \frac{k+1}{L-1} \; 1 \le k \le L-2 \end{cases} \quad (6)$$

The proof of equation (6) is in appendix in [9], [12] and [13].

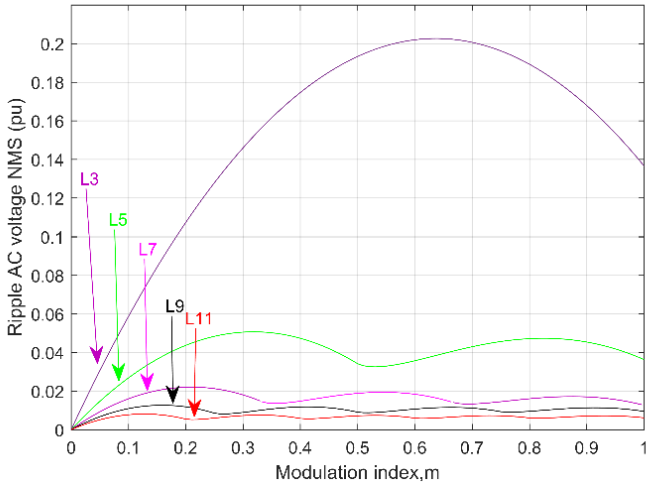

Fig. 7. NMS for H-Bridge AC PWM

Fig 7 shows NMS criterion for H-Bridge AC PWM for the same numbers of levels: 3, 5, 7, 9 and 11 as in fig 6.

Voltage Total Harmonic Distortion THD can be calculated for an arbitrary number of levels and by varying m according to sublevels as follows:

$$THD_L(m),\% = \frac{\sqrt{2NMS_L^{AC}(m)}}{m}.100\% \quad (7)$$

The voltage THD graphs are shown the same figures of the voltage THD graphs obtained with the second method.

IV. Simulation Of Thd (%) And Discussion

In the second method, the total harmonic distortion rate of the output voltage of the multilevel inverter is considered for comparison with the results obtained from (7) in the first method. For single-phase multilevel inverters, THD is a criterion for evaluating energy quality, especially if this energy is produced by a renewable energy source and injected into the electricity network. In accordance with the condition of the first method on the ratio between the fundamental frequency and the switching frequency, which must be greater than 20, the switching frequency is set at 1500Hz.

To extend the method to any number of voltage levels, taking into account the zero level, it is useful to use the relation L = 2n + 1, where n is the number of basic units or H-Bridges in series. The modulation index must vary in the same interval as in the first method, namely from 0.1 to 1. Also, it is entirely possible to apply this method to the different topologies already mentioned; Diode Clamped DCMLI and Flying Capacitor FCMLI.

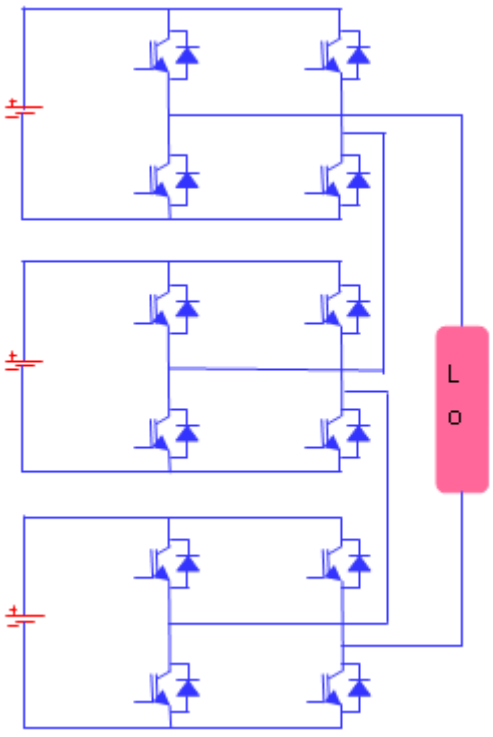

Fig. 8. Seven level CHB inverter topology

As an example, the 7-level multilevel inverter is shown in the figure 8 and well illustrates the ease offered by the base unit to connect the necessary number of H-Bridges in series to obtain the waveform of the desired output voltage.

The simulation was carried out for levels 3, 5, 7, 9 and 11 for a variation of the modulation rate from 0.1 to 1 with a step of 0.05. All THD values have been reported in Table 1.

Table I. Single Phase THD of CHB-MLI.

m	L				
	3	5	7	9	11
0.10	495.81	262.04	192.21	156.05	129.27
0.15	269.99	192.21	134.57	109.99	84.450
0.20	262.04	156.05	109.99	79.300	55.620
0.25	202.06	129.27	84.450	55.620	45.370
0.30	192.21	109.99	67.430	45.040	40.570
0.35	162.36	93.260	49.690	42.970	34.720
0.40	156.05	79.300	45.040	39.370	27.730
0.45	134.57	67.430	42.630	34.150	24.970
0.50	129.27	55.620	40.570	27.730	24.010
0.55	112.34	48.410	37.800	24.680	22.050
0.60	109.99	45.040	34.150	24.460	18.390
0.65	98.400	43.380	29.060	23.840	17.640
0.70	93.260	42.970	25.500	21.370	16.530
0.75	84.450	40.570	24.970	18.390	15.970
0.80	79.300	39.370	24.460	16.840	14.570
0.85	70.990	37.010	23.840	16.410	12.930
0.90	67.430	34.150	22.960	16.490	13.100
0.95	58.100	31.110	20.770	16.020	12.870
1.00	55.400	27.580	18.270	14.470	10.750

Fig 8 shows forms of carriers and reference signals for CHB PWM 7 level inverter. Index modulation is fixed to at m = 0.8, fundamental frequency f at 50Hz and switching frequency f_{cr} at 1000Hz. Carrier signals were level shifted in In-Phase Disposition (IPD).

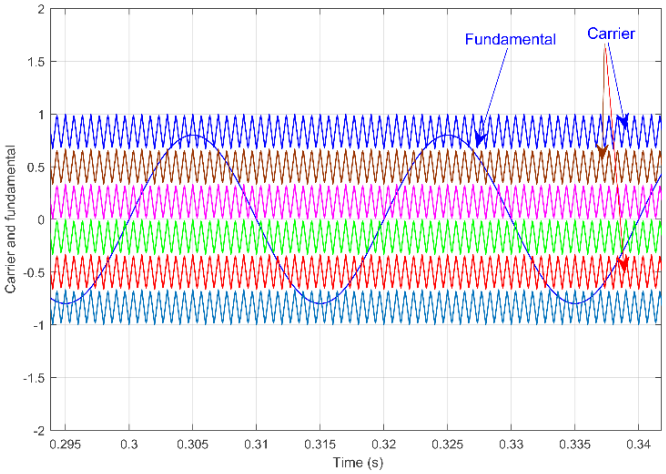

Fig. 9. Level-shifted multicarrier modulation for 7 level inverter

The figure 9 shows the simulation for L=7 which required 3 H-Bridges, and gives 7 voltage levels. As the DC voltage for each base unit is 100 V, the output voltage with the staircase form took the following values:
$V = 0V$; $V = \mp 100V$; $V = \mp 200V$; $V = \mp 300V$

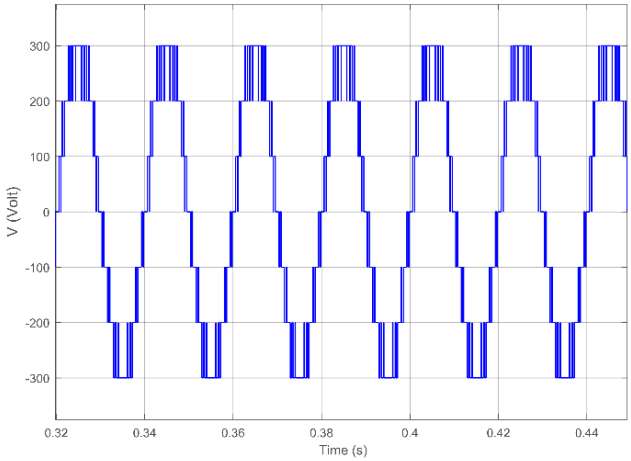

Fig. 10. Simulation result of output voltage for 7 levels

Figure 11 presents 4 graphs. Two of them illustrate the theoretical calculation and simulation of the total harmonic distortion THD for level 3 and the other two for level 5. We notice that the graphs relating to L3 correspond perfectly in the interval 0.5 to 1 but less well in the interval 0.1 to 0.4. It should be noted here that the theoretical graph is made in one piece. The theoretical graph of L5 is piecewise function. In the interval 0.5 to 1, the two graphs match perfectly while in the interval 0.1 to 0.5, the graphs match less well

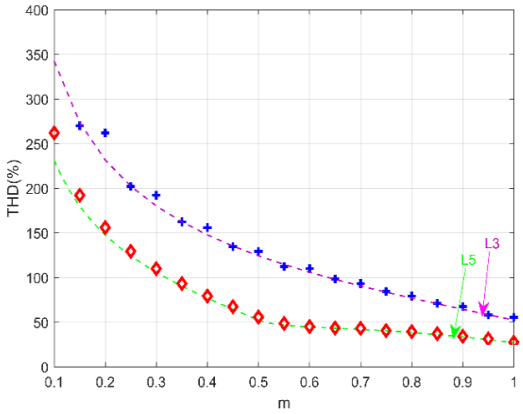

Fig. 11. Voltage THD (%) of single phase HBMLI for L=3,5

Figure 11 presents the graphs corresponding to levels L7, L9 and L11. The three theoretical graphs are piecewise function and correspond perfectly with the simulation graphs.

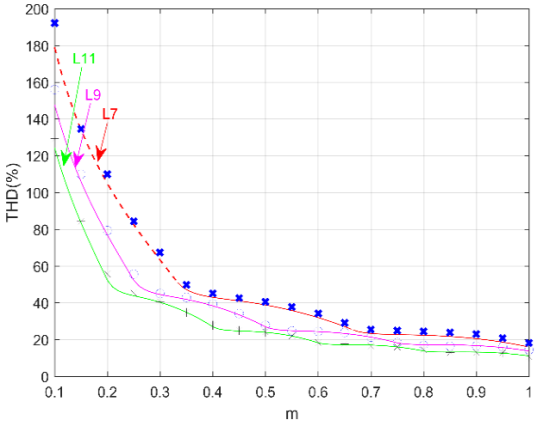

Fig. 12. Voltage THD (%) of single phase HBMLI for L=7,9 and 11 application to grid connected multilevel pwm inverter

The authors of reference [12] mention that if the ratio between the carriers and the fundamental frequency is greater than 15-20, the precision of the asymptotic formulas NMS-DC, NMS-AC and THD are acceptable. They added that for the fundamental frequency of 50 to 60 Hz, it would be sufficient for the switching frequency to be higher than only 1.0 to 1.2 kHz for good practical accuracy of the suggested formulas for voltage quality.

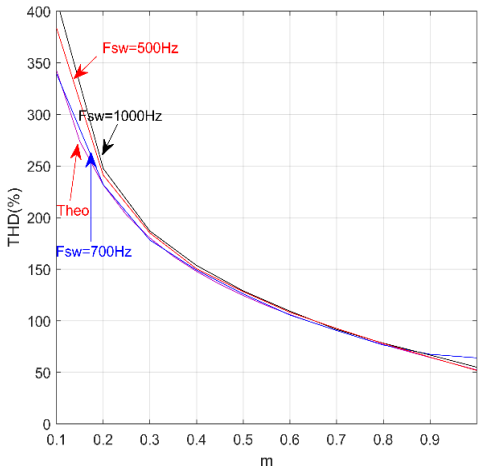

Fig. 13. Three level Voltage THD (%) of single phase HBMLI for fsw =500Hz, 1000Hz and 500Hz

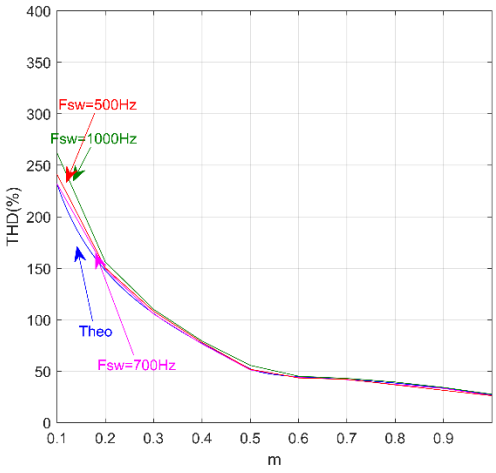

Fig. 14. Five level Voltage THD (%) of single phase HBMLI for fsw =500Hz, 1000Hz and 500Hz

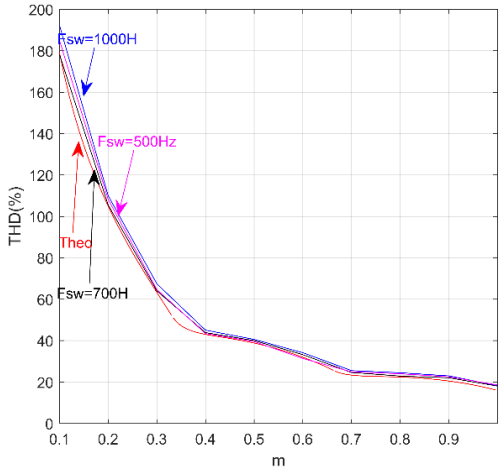

Fig. 15. Seven level Voltage THD (%) of single phase HBMLI for fsw =500Hz, 1000Hz and 500Hz

In this work, a comparison between the THD results for the voltage levels already discussed; L=3, 5, 7, 9 and 11 for three different cutoff frequency values: 700 Hz, 1000 Hz and 500 Hz. The choice of the 700Hz value is made based on the ratio between carriers and fundamental frequency (15-20) given in[12], which almost corresponds to the minimum value (15). After simulating with this value, it makes sense to check for a higher value (1000Hz) and another lower value (500Hz).

The results show, contrary to the values given in [12], that the cutoff frequency fsw=700Hz gave better agreement between the simulation and the theoretical values as shown in Figures 13, 14 and 15.

It should be noted that there is no significant difference in THD for the considered frequencies in the interval 0.3 to 1 of the modulation index. Furthermore, for modulation indices of 0.1 to 0.4, the simulation clearly shows the superiority in the accuracy of the chosen switching frequency (700Hz).

It can be concluded that this method gives better results for the number of voltage levels quite high because in general, the modulation index does not take small values, especially in the case of the shift level because the reference signal does not intersect with all carrier signals.

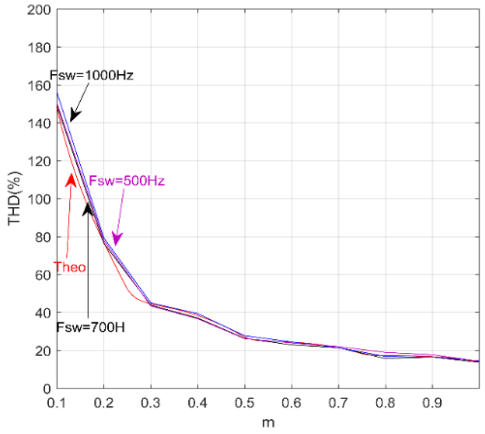

Fig. 16. Nine level Voltage THD (%) of single phase HBMLI for fsw =500Hz, 1000Hz and 500Hz

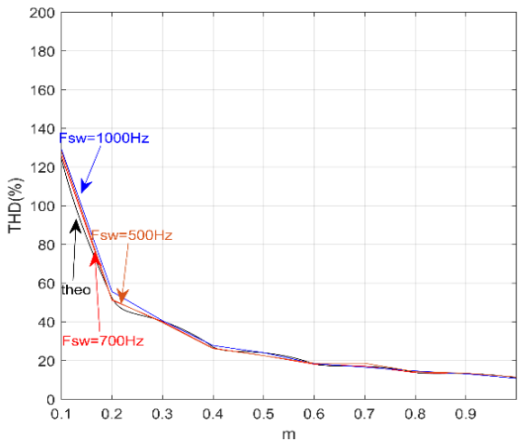

Fig. 17. Eleven level Voltage THD (%) of single phase HBMLI for fsw =500Hz, 1000Hz and 500Hz

V. CONCLUSION

The approach proposed in references [12-14] which consists of evaluating the output voltage quality of the multilevel PWM inverter in the time domain turned out to be simpler than the evaluation of the voltage in the frequency domain which requires a double expansion in Fourier series and considerable execution time. The calculation carried out by this theoretical method made it possible to evaluate the total harmonic distortion THD for odd order levels; 3, 5, 7, 9 and 11 by varying the modulation index from 0.1 to 1. The results made it possible to draw curves which are compared with curves obtained from the second method which consisted of simulating in Matlab/Simulink the model of the CHB-PWM multilevel inverter for the different levels studied and the same interval of the modulation index. The comparison shows that both methods gave curves that matched reasonably well for arbitrary voltage levels and the cited range of modulation index. A third factor may also be involved: the switching frequency.

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