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Asymmetrically Switched Modular CHB Inverters with High Frequency Control for Grid-Tied and Stand-Alone Applications

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Abstract: - Sinusoidal pulse width modulation (SPWM) techniques are commonly utilized in traditional multilevel inverter (MLI) designs through multi-carrier integration. This paper introduces an asymmetrically switched Cascaded H-Bridge MLI (CHBMLI) using multi-carrier pulse width modulation (MCPWM) control methods. The proposed CHB topology accommodates various DC input source configurations. Boolean algebra and logic simplifications are applied to design the switching inputs for each asymmetrical structure. This identifies control logics for all possible asymmetrical switching scenarios. This design reduces switch count and enhances power quality. The asymmetrical inverter is simulated with both resistive and inductive loads, and the 9 and 27-level trinary CHBMLI is further modeled for grid-tied power generation. Simulation results are validated through Hardware-in-the-Loop (HIL) testing, confirming the inverter's feasibility and Total Harmonic Distortion (THD) performance. As a multistring inverter, this topology is ideal for solar energy integration, including both standalone and grid-tied operation.

Keywords: CHB Multilevel Inverters, MCPWM Control, Asymmetrical Switching, Total Harmonic Distortion (THD), Grid-Tied Power Generation, Stand-Alone Application, Hardware-in-the Loop (HIL).

I. INTRODUCTION

Conventional multilevel inverters are namely (1) diode clamped (DCMLI) [1, 2], (2) flying capacitor (FCMLI) [3, 4] and (3) cascaded H bridge (CHBMLI) [5]. The advantage of using DCMLI or FCMLI is the requirement of single-sourced, but they have a great limitation because the increase in the number of levels they incorporate large component counts. On the other hand, CHB topology has fewer component counts concerning other classical topologies, but it needs separate dc sources [6]. Although it seems to be a limitation of requiring more than one dc source, it is permission for renewable energy researchers, especially solar and wind power application researchers, to integrate these energy sources using CHB topologies [7, 8]. A combination of symmetrical and asymmetrical sources may produce different output voltage levels, mainly increased output voltage with asymmetrical sources. CHB inverter has this provision to cause a different level of the output voltage by using asymmetrical inputs sources with lower component counts. Besides, asymmetrical switching of CHB inverters reduces the component count of MLI design, improves system efficiency, and reduces the size of the inverter [9-11]. Moreover, switching redundancy is available in CHB inverter topology. Both the additive and subtractive switching can also generate required output levels, which is also an attractive feature of this topology [12]. According to DC sources input, there are four asymmetrical switching techniques possible for CHB inverter (1) Natural sequence MLI (NSMLI), (2) Binary MLI (BMLI), (3) Trinary MLI (TMLI), and (4) Quasilinear MLI (QLMLI). For NSMLI, the input dc sources are applied considering the arithmetic progression, where the first element and common difference one. In the case of BMLI and THLI, dc sources are applied through a geometric progression of first term one and common ratios of two and three respectively. QLMLI is designed with non- uniform but constant progression to achieve required and specified level [13]. In this work, a scaled version of NSMLI, BMLI, QLMLI, and TMLI are considered to implement the MCPWM technique.

The switching strategy of multilevel inverters is generally two types. One is low frequency based switching, also called fundamental switching; another one is high frequency-based. Low frequency-based switching techniques may be incorporated either offline or online calculations to meet specific applications [14]. For offline calculation, the easiest method of switching angles estimation is an analytical method where the angles are calculated using a numerical formula for the first quadrant considering quarter-wave symmetry of multilevel waveform [15, 16]. Another method is the nearest vector control, where the reference vector is compared with the actual vector to minimize the error to generate a specific output level. The nearest level control technique is also used to generate the required level by comparing reference and actual voltage levels [17, 18]. Both the cases, lower-order harmonics are present, and to eliminate the lower order harmonics properly, SHE- PWM methods are used where SHE- PWM equations are solved using numerical or optimization techniques. There are different types of SHE- PWM techniques used: NR method, resultant

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theory, GA, PSO, etc. Every method has its pros and cons respectively. Generally, for online switching techniques, ANN or some bioinspired algorithms are used for required applications [19].

High-frequency switching mainly concentrates on either reference-based modulation or carrier-based approach. In reference-based modulation, only the reference signal is different and varied, such as Sinusoidal PWM, Trapezoidal PWM, 60^0 PWM, Third Harmonic Injection PWM, staircase modulation, hybrid reference, and discontinuous reference, etc. Here all the references are selected for a particular application with some special provisions. For example, in third harmonic injection PWM, the amplitude of the fundamental output voltage is 15% greater than the reference voltage. THD is always sacrificed because of reference selection in the design. Another method is Space Vector Modulation (SVM), which is used by different researchers to reduce the switching losses but not suitable for high-level design as it generates switching system complexity with the increase of the number of output levels [20, 21]. The carrier-based approach can be subdivided into two parts one is level shift PWM (LSPWM), and another one is phase shift PWM (PSPWM). LSPWM is further classified as an equal frequency and unequal frequency method. Equal frequency methods are phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD), carrier overlapping, and variable amplitude & hybrid techniques. In the case of an unequal or variable frequency method, all the carrier frequency is not the same and selected to adjust the specific levels to be generated. PSPWM techniques are mainly applicable for reducing the output power distortion for specified level design [22, 23].

Essentially, the losses of MLI depends on switching frequency range and types of carriers used. Three LSPWM based MCPWM techniques are the most commonly used to control the switching strategy of multilevel inverters, i.e., phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD). In the case of PD, all the carriers, including upper and lower of time coordinate, are in phase. For POD, lower carriers are out of phase with upper carriers, and for APOD, consecutive carriers are 180 phase-shifted at both upper and lower portion of the time axis. In this paper, PD, POD, and APOD based switching are considered as an MCPWM technique [24].

In the MCPWM control technique with symmetrical switching for CHB inverter where all the dc sources are equal, the switch logic design is simple as the number of carriers and the number of switches maintain a linear relationship multiplied by 2. For example, m level design number of total carriers required (m-1) and the number of switches required is 2(m-1). But for asymmetrical switching, it is not at all maintain a linear relationship like symmetrical switching. For this reason, it is challenging for the researchers to design switch logic for asymmetrical switching as the number of carriers increased rapidly with respect to the number of switches.

Boolean expressions are an effective tool for designing switch logic for asymmetrically switched MLI and MLI with reduced switch count. Normally three basic gates AND, OR, and NOT are used to design switch logic for the complementary situation. But for critical cases, exclusive operations, i.e., XOR ($\oplus$) and XNOR (), need to be considered. Also, there are two universal gates NAND & NOR are available by using the basic and exclusive gates can be implemented easily. This switch logic development method is relatively tricky and matter of patience as complexity arises and grows rapidly with the increase of the number of levels and carriers. All types of Boolean functions and their truth table including logic diagrams discussed in brief in the basic textbook of digital electronics. [25, 26].

After an extensive literature review, it is visualized that minimal reference is available about the switch logic expressions for the MCPWM strategy for asymmetric switched CHBMLI design. For the advantages mentioned above, MCPWM based switching and control techniques are proposed for asymmetrically switched CHB inverter topology by developing switch inputs through logic algebra or Boolean implementation, including modular expressions. The proposed inverters are suitable for renewable power generation, especially off-grid and on-grid Photovoltaic applications, as specified by different codes and standards [27-29]. Authors' contribution mainly focused on the development of-

- Different types of modular CHB converters with their symmetrical and asymmetrical modulation and control strategies.
- Achievement of different levels by using PD, POD, APOD control techniques.
- Hardware in the Loop implementation of the proposed asymmetrical switching.

- Grid-tied and standalone application results are shown to prove the feasibility of the proposed control strategies.

II. BASIC CHB INVERTER TOPOLOGY AND MODULATION

Figure 1(a) reveals the conventional CHB inverter topology with a scaled version for m level design and n number switches. Usually, it has s number of dc sources or H bridge modules, and each module is cascaded to form m levels through different combinations of H bridge switches. This CHB inverter can be engaged for the generation of required levels by applying equal or unequal dc sources. Considering symmetrical and asymmetrical dc inputs to the proposed inverter, the following source arrangements can be specified [13].

- Symmetrical MLI or CHBMLI- ($V_1=V_2=V_3=\ldots\ldots=V_s=V$)
- Asymmetrical NSMLI or CHBNSMLI- ($V_1=V$, $V_2=2V$, $V_3=3V$, ……, $V_s=sV$)
- Asymmetrical BMLI or CHBBMLI- ($V_1=V$, $V_2=2V$, $V_3=4V$, ,……, $V_s=2^{(s-1)}V$)
- Asymmetrical QLMLI or CHBQLMLI- ($V_1=V$, $V_2=2V$, $V_3=3V$,……, Vs= (4s-6) V)
- Asymmetrical TMLI or CHBTMLI- ($V_1=V$, $V_2=3V$, $V_3=9V$, ……, $V_s=3^{(s-1)}V$)

It is to be mentioned here that $S_{(4n-3)}$ is always complementary to $S_{(4n-2)}$ for each H bridge. And $S_{(4n-1)}$ is complementary to S_{4n}.

Table 1 shows the maximum number of levels to be achieved by using symmetrical and asymmetrical source configurations. From Table 2, it can be articulated that CHBTMLI generates the maximum number of levels with an identical number of dc sources. Figure 1(b) shows the schematic diagram of the proposed inverter for the three input DC sources with asymmetrical configureations namely CHBNSMLI, CHBQLMLI, CHBBMLI, and CHBTMLI. This schematic diagram discloses the fact of asymmetrical switching input to design 7, 19, 15, and 27 level respectively.

Table 1: Calculation of the maximum number of level

Proposed MLI (symmetrical and asymmetrical)	Maximum number of levels
CHBMLI	2s+1
CHBNSMLI	s^2+s+1
CHBBMLI	$2\times2^s-1$
CHBQLMLI	$s^2+7s-11$
CHBTMLI	3^s

For the generation of switching states from the proposed topologies, let us consider two input sources or H bridges. The number of levels can be anticipated as 5, 7, 7, 7 & 9 respectively for CHBMLI, CHBNSMLI, CHBBMLI, CHBQLMLI, and CHBTMLI that can be arranged at Table 2, 3 & 4. If three input sources are considered, then the number of levels will be 7, 13, 15, 19 & 27, respectively, for consecutive cases. Table 5, 6, 7, 8 & 9 display the switching states for 7, 13, 15, 19 & 27 level design considering three H bridges.

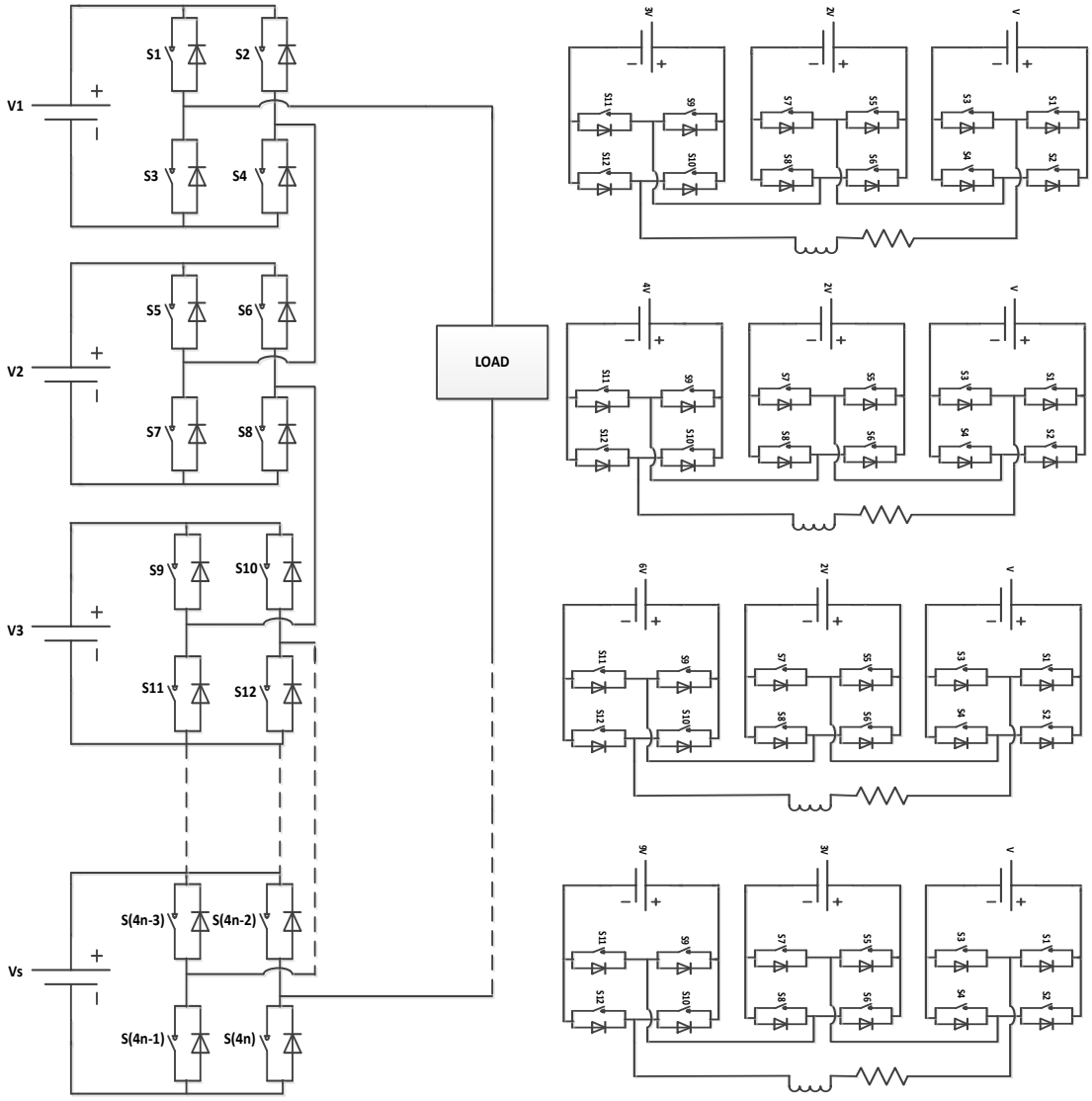
Table 2: Switching states for 5 level (2 H bridges), $V_1= V_2= V$

Switching States	**Output Voltage (Volts)**
S_1,S_4, S_8	V_1 (V)
S_1, S_4, S_5, S_8	$V_1+ V_2$ (2V)
S_1, S_2, S_5, S_6	0
S_2, S_3, S_7	-V_1 (-V)
S_2, S_3, S_6, S_7	-($V_1+ V_2$) (-2V)

Table 3: Switching states for 7 level (2 H bridges), $V_1= V$ &$V_2= 2V$

Switching States	**Output Voltage (Volts)**
S_1, S_4, S_8	V_1 (V)
S_4, S_5, S_8	V_2 (2V)
S_1, S_4, S_5, S_8	$V_1+ V_2$ (3V)
S_1, S_2, S_5, S_6	0

S_2, S_3, S_7	$-V_1$ (-V)
S_3, S_6, S_7	$-V_2$ (-2V)
S_2, S_3, S_6, S_7	-(V_1+ V_2) (-3V)



(a) (b)

Figure 1: CHB inverter topology (a) basic structure (b) schematic diagram for the different asymmetrical inputs.

Table 4: Switching states for 9 level (2 H bridges), V_1= V &V_2= 3V

Switching States	**Output Voltage (Volts)**
S_1, S_4, S_8	V_1 (V)
S_2, S_3, S_5, S_8	V_2- V_1 (2V)
S_4, S_5, S_8	V_2 (3V)
S_1, S_4, S_5, S_8	V_1+ V_2 (4V)
S_1, S_2, S_5, S_6	0
S_2, S_3, S_7	$-V_1$ (-V)
S_1, S_4, S_6, S_7	-(V_2- V_1) (-2V)
S_3, S_6, S_7	$-V_2$ (-3V)
S_2, S_3, S_6, S_7	-(V_1+ V_2) (-4V)

Table 5: Switching states for 7 level (3 H bridges), $V_1=V_2=V_3=V$

Switching States	Output Voltage (Volts)
S_1, S_4, S_8, S_{12}	V_1 (V)
$S_1, S_4, S_5, S_8, S_{12}$	$V_1+ V_2$ (2V)
$S_1, S_4, S_5, S_8, S_9, S_{12}$	$V_1+ V_2+ V_3$ (3V)
$S_1, S_2, S_5, S_6, S_9, S_{10}$	0
S_2, S_3, S_7, S_{11}	$-V_1$ (-V)
$S_2, S_3, S_6, S_7, S_{11}$	$-(V_1+ V_2)$ (-2V)
$S_2, S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_1+ V_2+ V_3)$ (-3V)

Table 6: Switching states for 13 level (3 H bridges), $V_1= V$, $V_2= 2V$ & $V_3=3V$

Switching States	Output Voltage (Volts)
S_1, S_4, S_8, S_{12}	V_1 (V)
S_4, S_5, S_8, S_{12}	V_2 (2V)
S_4, S_8, S_9, S_{12}	V_3 (3V)
$S_1, S_4, S_8, S_9, S_{12}$	V_1+V_3 (4V)
$S_4, S_5, S_8, S_9, S_{12}$	V_2+V_3 (5V)
$S_1, S_4, S_5, S_8, S_9, S_{12}$	$V_1+V_2+V_3$ (6V)
$S_1, S_2, S_5, S_6, S_9, S_{10}$	0
S_2, S_3, S_7, S_{11}	$-V_1$ (-V)
S_3, S_6, S_7, S_{11}	$-V_2$ (-2V)
S_3, S_7, S_{10}, S_{11}	$-V_3$ (-3V)
$S_2, S_3, S_7, S_{10}, S_{11}$	$-(V_1+V_3)$ (-4V)
$S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_2+V_3)$ (-5V)
$S_2, S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_1+V_2+V_3)$ (-6V)

Table 7: Switching states for 15 level (3 H bridges), $V_1= V$, $V_2= 2V$ & $V_3=4V$

Switching States	Output Voltage (Volts)
S_1, S_4, S_8, S_{12}	V_1 (V)
S_4, S_5, S_8, S_{12}	V_2 (2V)
$S_1, S_4, S_5, S_8, S_{12}$	V_1+V_2 (3V)
S_4, S_8, S_9, S_{12}	V_3 (4V)
$S_1, S_4, S_8, S_9, S_{12}$	V_1+V_3 (5V)
$S_4, S_5, S_8, S_9, S_{12}$	V_2+V_3 (6V)
$S_1, S_4, S_5, S_8, S_9, S_{12}$	$V_1+V_2+V_3$ (7V)
$S_1, S_2, S_5, S_6, S_9, S_{10}$	0
S_2, S_3, S_7, S_{11}	$-V_1$ (-V)
S_3, S_6, S_7, S_{11}	$-V_2$ (-2V)
$S_2, S_3, S_6, S_7, S_{11}$	$-(V_1+V_2)$ (-3V)
S_3, S_7, S_{10}, S_{11}	$-V_3$ (-4V)
$S_2, S_3, S_7, S_{10}, S_{11}$	$-(V_1+V_3)$ (-5V)
$S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_2+V_3)$ (-6V)
$S_2, S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_1+V_2+V_3)$ (-7V)

Table 8: Switching states for 19 level (3 H bridges), $V_1= V$, $V_2= 2V$ & $V_3=6V$

Switching States	Output Voltage (Volts)
S_1, S_4, S_8, S_{12}	V_1 (V)
S_4, S_5, S_8, S_{12}	V_2 (2V)
$S_2, S_3, S_6, S_7, S_9, S_{12}$	$V_3-V_2-V_1$ (3V)
$S_4, S_6, S_7, S_9, S_{12}$	V_3-V_2 (4V)
$S_2, S_3, S_8, S_9, S_{12}$	V_3-V_1 (5V)
S_4, S_8, S_9, S_{12}	V_3 (6V)
$S_1, S_4, S_8, S_9, S_{12}$	V_1+V_3 (7V)

$S_4, S_5, S_8, S_9, S_{12}$	V_2+V_3 (8V)
$S_1, S_4, S_5, S_8, S_9, S_{12}$	$V_1+V_2+V_3$ (9V)
$S_1, S_2, S_5, S_6, S_9, S_{10}$	0
S_2, S_3, S_7, S_{11}	$-V_1$ (-V)
S_3, S_6, S_7, S_{11}	$-V_2$ (-2V)
$S_1, S_4, S_5, S_8, S_{10}, S_{11}$	$-(V_3-V_2-V_1)$ (-3V)
$S_3, S_5, S_8, S_{10}, S_{11}$	$-(V_3-V_2)$ (-4V)
$S_1, S_4, S_7, S_{10}, S_{11}$	$-(V_3-V_1)$ (-5V)
S_3, S_7, S_{10}, S_{11}	$-V_3$ (-6V)
$S_2, S_3, S_7, S_{10}, S_{11}$	$-(V_1+V_3)$ (-7V)
$S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_2+V_3)$ (-8V)
$S_2, S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_1+V_2+V_3)$ (-9V)

Table 9: Switching states for 27 level (3 H bridges), V_1= V, V_2= 3V & V_3=9V

Switching States	**Output Voltage (Volts)**
S_1, S_4, S_8, S_{12}	V_1 (V)
$S_2, S_3, S_5, S_8, S_{12}$	V_2-V_1 (2V)
S_4, S_5, S_8, S_{12}	V_2 (3V)
$S_1, S_4, S_5, S_8, S_{12}$	V_1+V_2 (4V)
$S_2, S_3, S_6, S_7, S_9, S_{12}$	$V_3-V_2-V_1$ (5V)
$S_4, S_6, S_7, S_9, S_{12}$	V_3-V_2 (6V)
$S_1, S_4, S_6, S_7, S_9, S_{12}$	$V_3- V_2 +V_1$ (7V)
$S_2, S_3, S_8, S_9, S_{12}$	V_3-V_1 (8V)
S_4, S_8, S_9, S_{12}	V_3 (9V)
$S_1, S_4, S_8, S_9, S_{12}$	V_3+V_1 (10V)
$S_2, S_3, S_5, S_8, S_9, S_{12}$	$V_3+V_2-V_1$ (11V)
$S_4, S_5, S_8, S_9, S_{12}$	V_3+V_2 (12V)
$S_1, S_4, S_5, S_8, S_9, S_{12}$	$V_3+V_2+V_1$ (13V)
$S_1, S_2, S_5, S_6, S_9, S_{10}$	0
S_2, S_3, S_7, S_{11}	$-V_1$ (-V)
$S_1, S_4, S_6, S_7, S_{11}$	$-(V_2-V_1)$ (-2V)
S_3, S_6, S_7, S_{11}	$-V_2$ (-3V)
$S_2, S_3, S_6, S_7, S_{11}$	$-(V_1+V_2)$ (-4V)
$S_1, S_4, S_5, S_8, S_{10}, S_{11}$	$-(V_3-V_2-V_1)$ (-5V)
$S_3, S_5, S_8, S_{10}, S_{11}$	$-(V_3-V_2)$ (-6V)
$S_2, S_3, S_5, S_8, S_{10}, S_{11}$	$-(V_3- V_2 +V_1)$ (-7V)
$S_1, S_4, S_7, S_{10}, S_{11}$	$-(V_3-V_1)$ (-8V)
S_3, S_7, S_{10}, S_{11}	$-V_3$ (-9V)
$S_2, S_3, S_7, S_{10}, S_{11}$	$-(V_3+V_1)$ (-10V)
$S_1, S_4, S_6, S_7, S_{10}, S_{11}$	$-(V_3+V_2-V_1)$ (-11V)
$S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_3+V_2)$ (-12V)
$S_2, S_3, S_6, S_7, S_{10}, S_{11}$	$-(V_3+V_2+V_1)$ (-13V)

As already discussed MCPWM strategy in the introduction section, three different LSPWM is proposed. For PD, POD, and APOD, the output THD is varied because of changing carrier pattern. The output THD variation can also be realized by varying the Modulation Index (MI). The MI can be defined as the amplitude of the reference signal (A_R) upon the carrier signal (A_C). Another term is called a frequency ratio (FR), which is the frequency of the carrier signal (F_C) upon the frequency of the reference signal (F_R). The frequency ratio mainly discloses the harmonic amplitude, which is most significant with respect to the fundamental one.

III. Switch Logic Generation Methods

For the generation of switch logic in MCPWM based control techniques using quarter-wave symmetry approximation of multilevel inverters, the number of carriers under 'ON' & 'OFF' states is associated with switching ON & OFF states. Fundamentally, for m level design, (m-1) carriers are required where the number of positive and negative carriers is (m-1)/2, respectively. For m level design, how positive and negative carriers are distributed, as shown in Figure 2. Here, P_1, P_2, P_3,……., $P_{(m-1)/2}$ are positive carriers & N_1, N_2, N_3,……..., $N_{(m-1)/2}$ are the negative carriers. The nth term of positive and negative carriers is equal to (m-1)/2, i.e., n= (m-1)/2 for each design.

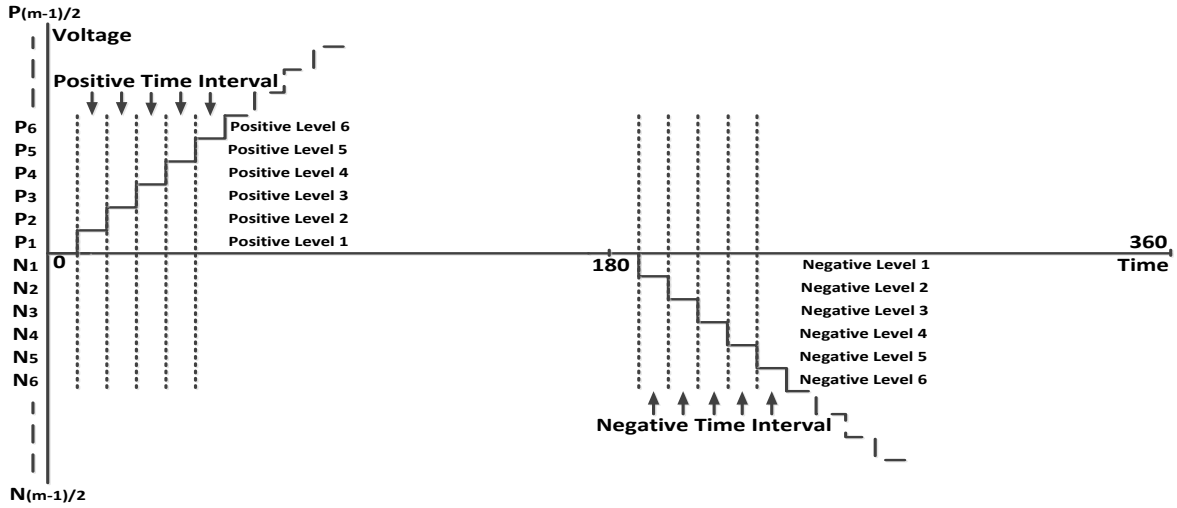


Figure 2: Carrier distribution for m level design

For example, how positive and negative carriers are distributed to switch inputs is the primary concern of this work. If two H Bridges are considered with symmetrical (CHBMLI) 5 level design, eight switches and four carriers are required. The logical expressions can be established for all the switches in 5 level design through the following equations (1) to (3)-

$$S_1, S_4, S_8=P_1 \quad (1)$$

$$S_2, S_3, S_7=N_1^{/} \quad (2)$$

$$S_5=P_2, S_6=N_2^{/} \quad (3)$$

Similarly, the control logic for switch inputs to symmetrical 7 level design with three H bridges can be stated as equations (4) to (7) according to Table 6. It has 12 switches and six carriers.

$$S_1, S_4, S_8, S_{12}=P_1 \quad (4)$$

$$S_2, S_3, S_7, S_{11}=N_1^{/} \quad (5)$$

$$S_5=P_2, S_6=N_2^{/} \quad (6)$$

$$S_9=P_3, S_{10}=N_3^{/} \quad (7)$$

The logical expressions for symmetrical m level design can also be presented through equations (8) to (11).

$$S_1=P_1, S_5=P_2, S_9=P_3, S_{13}=P_4, = \ldots\ldots\ldots, = S_{4n-3}=P_{(m-1)/2} \quad (8)$$

$$S_2=N_1^{/}, S_6=N_2^{/}, S_{10}=N_3^{/}, S_{14}=N_4^{/}, = \ldots\ldots\ldots, = S_{4n-2}=N_{(m-1)/2}^{/} \quad (9)$$

$$S_3=N_1^{/}, S_7=N_1^{/}, S_{11}=N_1^{/}, S_{15}=N_1^{/}, = \ldots\ldots\ldots, = S_{4n-1}=N_1^{/} \quad (10)$$

$$S_4=P_1, S_8=P_1, S_{12}=P_1, S_{16}=P_1, = \ldots\ldots\ldots, = S_{4n}=P_1 \quad (11)$$

IV. CONTROL LOGIC FOR ASYMMETRICAL SWITCHING

In this section, logical equations for all types of asymmetrical switching are elaborated including their modular version of the control strategy for each category. Control logics are the same for asymmetrical 7 level design with two H bridges in CHBNSMLI, CHBBMLI & CHBQLMLI.

A. Control Logic for CHBNSMLI Design

If two H bridges are considered, then 7 level design is possible with six carriers. These six carriers are distributed to switch input by following logical operations, exp. (12) to (15).

$$S_1=(P_1 \oplus P_2) + P_3, S_2=(N_1' \oplus N_2')+N_3' \quad (12)$$
$$S_3=N_1', S_4=P_1 \quad (13)$$
$$S_5=P_2, S_6=N_2' \quad (14)$$
$$S_7=N_1', S_8=P_1 \quad (15)$$

It requires 12 carriers when three H bridges are considered & 13 levels are designed and implemented with the following control expressions (16) to (19)-

$$S_1=(P_1 \oplus P_2) + (P_4 \oplus P_5) + P_6, S_2=(N_1' \oplus N_2')+(N_4' \oplus N_5') + N_6' \quad (16)$$
$$S_5=(P_2 \oplus P_3) + P_5, S_6=(N_2' \oplus N_3')+N_5' \quad (17)$$
$$S_9=P_3, S_{10}=N_3' \quad (18)$$
$$S_4, S_8, S_{12}=P_1, S_3, S_7, S_{11}=N_1' \quad (19)$$

By using four H bridges, 21 level inverters can be designed that needs 20 carriers. The control logics are given below, equations (20) to (24)-

$$S_1=(P_1 \oplus P_2) + (P_5 \oplus P_6) + (P_8 \oplus P_9) + P_{10}, \quad (20)$$
$$S_2=(N_1' \oplus N_2')+(N_5' \oplus N_6') + (N_8' \oplus N_9')+N_{10}'$$
$$S_5=(P_2 \oplus P_3) + (P_6 \oplus P_7) + P_9, S_6=(N_2' \oplus N_3')+(N_6' \oplus N_7') + N_9' \quad (21)$$
$$S_9=(P_3 \oplus P_4) + P_7, S_{10}=(N_3' \oplus N_4')+N_7' \quad (22)$$
$$S_4, S_8, S_{12}, S_{16}=P_1, S_3, S_7, S_{11}, S_{15}=N_1' \quad (23)$$
$$S_{13} = P_4, S_{14} = N_4' \quad (24)$$

For m level design with s number of dc sources or H bridges following expressions can be produced as a scaled version in CHBNSMLI.

$$S_1=(P_1 \oplus P_2) + (P_4 \oplus P_5) + (P_5 \oplus P_6)+\ldots\ldots\ldots+P_{(m-1)/2} \quad (25)$$
$$S_5=(P_2 \oplus P_3) + (P_6 \oplus P_7)+\ldots\ldots\ldots+P_{(m-3)/2}$$
$$S_9=(P_3 \oplus P_4)+\ldots\ldots\ldots+P_{(m-7)/2}$$
. . .
. . .
. . .
$$S_{4n-3}=P_{[(8m-6)-\sqrt{2}]/2\sqrt{2}}$$
$$S_2=(N_1' \oplus N_2')+(N_4' \oplus N_5') + (N_5' \oplus N_6')+\ldots\ldots\ldots+N_{(m-1)/2}' \quad (26)$$
$$S_6=(N_2' \oplus N_3')+(N_6' \oplus N_7')+\ldots\ldots\ldots+N_{(m-3)/2}'$$
$$S_{10}=(N_3' \oplus N_4')+\ldots\ldots\ldots+N_{(m-7)/2}'$$
. . .
. . .
. . .
$$S_{4n-2} = N_{[(8m-6)-\sqrt{2}]/2\sqrt{2}}'$$
$$S_{4n-1}=N_1', S_{4n}=P_1 \quad (27)$$

B. Control Logic for CHBBMLI Design

Asymmetrical 7 level design with two H bridges, six carriers are required as already shown in expressions (12) to (15). For 15 level design, it requires 14 carries and three H bridges. The switching states are implemented with the corresponding logical expressions for 15 level design that can be termed by a successive set of equations from (28) to (31).

$$S_1=(P_1 \oplus P_2) + (P_3 \oplus P_4) + (P_5 \oplus P_6) + P_7, \quad (28)$$
$$S_2=(N_1^{/} \oplus N_2^{/})+(N_3^{/} \oplus N_4^{/}) + (N_5^{/} \oplus N_6^{/}) + N_7^{/}$$
$$S_5=(P_2 \oplus P_4) + P_6, S_6=(N_2^{/} \oplus N_4^{/})+N_6^{/} \quad (29)$$
$$S_9=P_4, S_{10}=N_4^{/} \quad (30)$$
$$S_4, S_8, S_{12}=P_1, S_3, S_7, S_{11}=N_1^{/} \quad (31)$$

Now for 31 level design, 30 carriers and four H bridges are required. The switch control input for each switch are shown below, where 30 carriers are merged with 16 switches critically.

$$S_1=(P_1 \oplus P_2)+(P_3 \oplus P_4)+(P_5 \oplus P_6)+(P_7 \oplus P_8)+ \quad (32)$$
$$(P_9 \oplus P_{10})+(P_{11} \oplus P_{12})+(P_{13} \oplus P_{14})+P_{15}$$
$$S_2=(N_1^{/} \oplus N_2^{/})+(N_3^{/} \oplus N_4^{/})+(N_5^{/} \oplus N_6^{/})+(N_7^{/} \oplus N_8^{/})$$
$$+ (N_9^{/} \oplus N_{10}^{/})+(N_{11}^{/} \oplus N_{12}^{/})+(N_{13}^{/} \oplus N_{14}^{/})+N_{15}^{/}$$
$$S_5=(P_2 \oplus P_4) + (P_6 \oplus P_8) + (P_{10} \oplus P_{12}) + P_{14}, \quad (33)$$
$$S_6=(N_2^{/} \oplus N_4^{/})+(N_6^{/} \oplus N_8^{/}) + (N_{10}^{/} \oplus N_{12}^{/})+N_{14}^{/}$$
$$S_9=(P_3 \oplus P_4) + P_7, S_{10}=(N_3^{/} \oplus N_4^{/})+N_7^{/} \quad (34)$$
$$S_4, S_8, S_{12}, S_{16}=P_1, S_3, S_7, S_{11}, S_{15}=N_1^{/} \quad (35)$$
$$S_{13} = P_8, S_{14} = N_8^{/} \quad (36)$$

If the modular form of control algorithm for CHBBMLI needs to be considered, then subsequent equations are considered at m level design with s number of H bridges.

$$S_1=(P_1 \oplus P_2) + (P_3 \oplus P_4) + (P_5 \oplus P_6)+\ldots\ldots+P_{(m-1)/2} \quad (37)$$
$$S_5=(P_2 \oplus P_4) + (P_6 \oplus P_8)+(P_{10} \oplus P_{12})\ldots\ldots+P_{(m-3)/2}$$
$$S_9=(P_4 \oplus P_8)+\ldots\ldots+P_{(m-7)/2}$$
. . .
. . .
. . .
$$S_{4n-3}=P_{(m+1)/4}$$
$$S_2=(N_1^{/} \oplus N_2^{/})+(N_3^{/} \oplus N_4^{/}) + (N_5^{/} \oplus N_6^{/})+\ldots\ldots+N_{(m-1)/2}^{/} \quad (38)$$
$$S_6=(N_2^{/} \oplus N_4^{/})+(N_6^{/} \oplus N_8^{/})+(N_{10}^{/} \oplus N_{12}^{/})\ldots\ldots+N_{(m-3)/2}^{/}$$
$$S_{10}=(N_4^{/} \oplus N_8^{/})+\ldots\ldots+N_{(m-7)/2}^{/}$$
. . .
. . .
. . .
$$S_{4n-2} = N_{(m+1)/4}^{/}$$
$$S_{4n-1}=N_1^{/}, S_{4n}=P_1 \quad (39)$$

C. Control Logic Design for CHBQLMLI Desin

Logical terminologies for two H bridges with 7 level is as like as previous. Now, it needs 18 carrier signals and three H bridges to design 19 levels according to dc source patterns. The expressions for 19 level design as exposed below in equations (40) to (45). Here analytically 18 carriers are merged with 12 switches.

$$S_1=[(P_1 \oplus P_2) + (P_3 \oplus P_4) + (P_7 \oplus P_8) + P_9] + (N_5 \oplus N_6) \quad (40)$$
$$S_2=[(N_1^{/} \oplus N_2^{/})+(N_3^{/} \oplus N_4^{/}) + (N_7^{/} \oplus N_8^{/}) + N_9^{/}]+(P_5 \oplus P_6)$$
$$S_4=[(P_1 \oplus P_5) + P_6] + (N_5 \oplus N_6) \quad (41)$$

$S_3=[(N_1^{/}\oplus N_5^{/})+N_6^{/}]+(P_5 \oplus P_6)$

$S_5=[(P_2 \oplus P_4) + P_8] + (N_4 \oplus N_5)$ (42)

$S_6=[(N_2^{/}\oplus N_4^{/})+N_8^{/}]+(P_4 \oplus P_5)$

$S_8=[(P_1 \oplus P_4) + P_5] + (N_4 \oplus N_5)$ (43)

$S_7=[(N_1^{/}\oplus N_4^{/})+N_5^{/}]+(P_4 \oplus P_5)$

$S_9=P_4$, $S_{10}=N_4^{/}$ (44)

$S_{12}=P_1$, $S_{11}=N_1^{/}$ (45)

33 level inverter can be designed with four H bridges in case of CHBQLMLI. To generate switch input logic properly, 32 carriers are required, and carrier merging is complicated in this design, as revealed below.

$S_1=[(P_1\oplus P_2)+(P_4\oplus P_5)+(P_6\oplus P_7)+(P_{11}\oplus P_{12})+(P_{14}\oplus P_{15})+P_{16}]+(N_9^{/}\oplus N_{10}^{/})$ (46)

$S_2=[(N_1^{/}\oplus N_2^{/})+(N_4^{/}\oplus N_5^{/})+(N_6^{/}\oplus N_7^{/})+(N_{11}^{/}\oplus N_{12}^{/})+(N_{14}^{/}\oplus N_{15}^{/})+N_{16}^{/}]+(P_9\oplus P_{10})$

$S_4=[(P_1 \oplus P_9) + P_{10}] +(N_9^{/}\oplus N_{10}^{/}$, $S_3=[(N_1^{/}\oplus N_9^{/})+N_{10}^{/}]+(P_9\oplus P_{10})$ (47)

$S_5=[(P_2 \oplus P_3) + (P_5 \oplus P_7) + (P_{12} \oplus P_{13}) + P_{15}] +(N_8^{/}\oplus N_9^{/})$ (48)

$S_6=[(N_2^{/}\oplus N_3^{/})+(N_5^{/}\oplus N_7^{/}) + (N_{12}^{/}\oplus N_{13}^{/})+N_{15}^{/}]+(P_8\oplus P_9)$

$S_8=[(P_1 \oplus P_8) + P_9]+(N_8^{/}\oplus N_9^{/})$, $S_7=[(N_1^{/}\oplus N_8^{/})+N_9^{/}]+(P_8\oplus P_9)$ (49)

$S_9=[(P_3 \oplus P_7) + P_{13}]+(N_7^{/}\oplus N_8^{/})$, $S_{10}=[(N_3^{/}\oplus N_7^{/})+N_{13}^{/}]+(P_7\oplus P_8)$ (50)

$S_{12}=[(P_1 \oplus P_7) + P_8]+(N_7^{/}\oplus N_8^{/})$, $S_{11}=[(N_1^{/}\oplus N_7^{/})+N_8^{/}]+(P_7\oplus P_8)$ (51)

$S_{13} = P_7, S_{14} = N_7^{/}$ (52)

$S_{16}=P_1$, $S_{15}=N_1^{/}$ (53)

For m level design, the scaled version is developed through the previous method with s number of sources for CHBQLMLI.

$S_1=[(P_1 \oplus P_2)+\cdots\cdots+P_{(m-1)/2}] +[N_{2\sqrt{(4m+93)}-19} \oplus N_{2\sqrt{(4m+93)}-20}]$ (54)

$S_5=[(P_2 \oplus P_3)+\cdots\cdots+P_{(m-3)/2}]+[N_{2\sqrt{(4m+93)}-18} \oplus N_{2\sqrt{(4m+93)}-19}]$

$S_9=[(P_3 \oplus P_7)+\cdots\cdots+P_{(m-7)/2}]+[N_{2\sqrt{(4m+93)}-17} \oplus N_{2\sqrt{(4m+93)}-18}]$

. . .

. . .

. . .

$S_{4n-3}=P_{[(m+41)-4\sqrt{(4m+93)}]/2}$

$S_2=[(N_1^{/}\oplus N_2^{/})+\cdots\cdots+N_{(m-1)/2}^{/}]+[P_{2\sqrt{(4m+93)}-19} \oplus P_{2\sqrt{(4m+93)}-20}]$ (55)

$S_6=[(N_2^{/}\oplus N_3^{/})+\cdots\cdots+N_{(m-3)/2}^{/}] +[P_{2\sqrt{(4m+93)}-18} \oplus P_{2\sqrt{(4m+93)}-19}]$

$S_{10}=[(N_3^{/}\oplus N_7^{/})+\cdots\cdots+N_{(m-7)/2}^{/}] +[P_{2\sqrt{(4m+93)}-17} \oplus P_{2\sqrt{(4m+93)}-18}]$

. . .

. . .

. . .

$S_{4n-2} = N_{[(m+41)-4\sqrt{(4m+93)}]/2}^{/}$

$S_3=[(N_1^{/}\oplus\cdots\cdots N_{2\sqrt{(4m+93)}-21}^{/})+N_{2\sqrt{(4m+93)}-20}^{/}]+[P_{2\sqrt{(4m+93)}-19} \oplus P_{2\sqrt{(4m+93)}-20}]$ (56)

$S_7=[(N_2^{/}\oplus\cdots\cdots N_{2\sqrt{(4m+93)}-22}^{/})+N_{2\sqrt{(4m+93)}-21}^{/}] +[P_{2\sqrt{(4m+93)}-18} \oplus P_{2\sqrt{(4m+93)}-19}]$

$S_{11}=[(N_3^{/}\oplus\ldots\ldots\ldots N^{/}_{2\sqrt{(4m+93)}-23})+N^{/}_{2\sqrt{(4m+93)}-22}] +[P_{2\sqrt{(4m+93)}-17} \oplus P_{2\sqrt{(4m+93)}-18}]$

. . .

. . .

. . .

$S_{4n-1}=N_1^{/}$

$S_4=[(P_1 \oplus \ldots\ldots\ldots P_{2\sqrt{(4m+93)}-21})+P_{2\sqrt{(4m+93)}-20}] +[N_{2\sqrt{(4m+93)}-19} \oplus N_{2\sqrt{(4m+93)}-20}]$ (57)

$S_8=[(P_2 \oplus \ldots\ldots\ldots P_{2\sqrt{(4m+93)}-22}) +P_{2\sqrt{(4m+93)}-21}]+[N_{2\sqrt{(4m+93)}-18} \oplus N_{2\sqrt{(4m+93)}-19}]$

$S_{12}=[(P_3 \oplus \ldots\ldots\ldots P_{2\sqrt{(4m+93)}-23})+P_{2\sqrt{(4m+93)}-22}]+[N_{2\sqrt{(4m+93)}-17} \oplus N_{2\sqrt{(4m+93)}-18}]$

. . .

. . .

. . .

$S_{4n}=P_1$

D. Control Logic for CHBTMLI Design

By using two H bridges, 9 level inverter can be generated with eight carriers for CHBTHMLI. The switching states are already provided in Table 3.

$S_1=[(P_1 \oplus P_2) + P_4] + (N_2 \oplus N_3)$ (58)

$S_2=[(N_1^{/}\oplus N_2^{/})+N_4^{/}]+(P_2 \oplus P_3)$

$S_4=[(P_1 \oplus P_2) + P_3] + (N_2 \oplus N_3)$ (59)

$S_3=[(N_1^{/}\oplus N_2^{/})+N_3^{/}]+(P_2 \oplus P_3)$

$S_5=P_2$, $S_6=N_2^{/}$ (60)

$S_8=P_1$, $S_7=N_1^{/}$ (61)

For the designing of 27 levels inverter, three H bridges are required with 26 carriers. The table associated with the switching states is provided in Table 4. The logical terms will be:-

$S_1=[(P_1 \oplus P_2) + (P_4 \oplus P_5) + (P_7 \oplus P_8) + (P_{10} \oplus P_{11}) + P_{13}]$ (62)
$+(N_2 \oplus N_3) + (N_5 \oplus N_6) + (N_8 \oplus N_9) + (N_{11} \oplus N_{12})$

$S_2=[(N_1^{/}\oplus N_2^{/})+(N_4^{/}\oplus N_5^{/}) + (N_7^{/}\oplus N_8^{/}) + (N_{10}^{/}\oplus N_{11}^{/}) + N_{13}^{/}]$
$+(P_2 \oplus P_3)+(P_5 \oplus P_6)+(P_8 \oplus P_9)+(P_{11} \oplus P_{12})$

$S_4=[(P_1 \oplus P_2) + (P_3 \oplus P_5) + (P_6 \oplus P_8) + (P_9 \oplus P_{11})+ P_{12}]$ (63)
$+(N_2 \oplus N_3) + (N_5 \oplus N_6) + (N_8 \oplus N_9) + (N_{11} \oplus N_{12})$

$S_3=[(N_1^{/}\oplus N_2^{/})+(N_3^{/}\oplus N_5^{/})+(N_6^{/}\oplus N_8^{/}) + (N_9^{/}\oplus N_{11}^{/}) + N_{12}^{/}]$
$+(P_2 \oplus P_3)+(P_5 \oplus P_6)+(P_8 \oplus P_9)+(P_{11} \oplus P_{12})$

$S_5=[(P_2 \oplus P_5) + P_{11}] + (N_5 \oplus N_8)$ (64)

$S_6=[(N_2^{/}\oplus N_5^{/})+N_{11}^{/}]+(P_5 \oplus P_8)$

$S_8=[(P_1 \oplus P_5) + P_8] + (N_5 \oplus N_8)$ (65)

$S_7=[(N_1^{/}\oplus N_5^{/})+N_8^{/}]+(P_5 \oplus P_8)$

$S_9=P_5$, $S_{10}=N_5^{/}$ (66)

$S_{12}=P_1$, $S_{11}=N_1^{/}$ (67)

By a similar fashion, the control logic for 81 level inverter can be elaborated by following equations (68) to (75). Here four H bridges are used where 80 carriers are merged judgmentally with 16 switches only.

$$S_1=[(P_1 \oplus P_2) + (P_4 \oplus P_5)+\ldots\ldots\ldots+P_{40}] + [(N_2 \oplus N_3) + (N_5 \oplus N_6)+\ldots\ldots\ldots+(N_{38} \oplus N_{39})] \quad (68)$$

$$S_2=[(N_1^{/}\oplus N_2^{/})+(N_4^{/}\oplus N_5^{/})+\ldots\ldots\ldots+N_{40}^{/}] + [(P_2 \oplus P_3) + (P_5 \oplus P_6)+\ldots\ldots\ldots+ (P_{38} \oplus P_{39})]$$

$$S_4=[(P_1 \oplus P_2) + (P_3 \oplus P_5)+\ldots\ldots\ldots+P_{39}] + [(N_2 \oplus N_3) + (N_5 \oplus N_6)+\ldots\ldots\ldots+(N_{38} \oplus N_{39})] \quad (69)$$

$$S_3=[(N_1^{/}\oplus N_2^{/})+(N_3^{/}\oplus N_5^{/})+\ldots\ldots\ldots+N_{39}^{/}] + [(P_2 \oplus P_3) + (P_5 \oplus P_6)+\ldots\ldots\ldots+ (P_{38} \oplus P_{39})]$$

$$S_5=[(P_2 \oplus P_5) + (P_{11} \oplus P_{14})+\ldots\ldots\ldots+P_{38}] + [(N_5 \oplus N_8) + (N_{14} \oplus N_{17})+\ldots\ldots\ldots+ N_{35}] \quad (70)$$

$$S_6=[(N_2^{/}\oplus N_5^{/})+(N_{11}^{/}\oplus N_{14}^{/})+\ldots\ldots\ldots+N_{38}^{/}] + [(P_5 \oplus P_8) + (P_{14} \oplus P_{17})+\ldots\ldots\ldots+ P_{35}]$$

$$S_8=[(P_1 \oplus P_5) + (P_8 \oplus P_{14})+\ldots\ldots\ldots+P_{35}] + [(N_5 \oplus N_8) + (N_{14} \oplus N_{17})+\ldots\ldots\ldots+ N_{35}] \quad (71)$$

$$S_7=[(N_1^{/}\oplus N_5^{/})+(N_8^{/}\oplus N_{14}^{/})+\ldots\ldots\ldots+N_{35}^{/}] + [(P_5 \oplus P_8) + (P_{14} \oplus P_{17})+\ldots\ldots\ldots+ P_{35}]$$

$$S_9=[(P_5 \oplus P_{14}) + P_{32}] + (N_{14} \oplus N_{23}) \quad (72)$$

$$S_{10}=[(N_5^{/}\oplus N_{14}^{/})+N_{32}^{/}]+(P_{14} \oplus P_{23})$$

$$S_{12}=[(P_1 \oplus P_{14}) + P_{23}] + (N_{14} \oplus N_{23}) \quad (73)$$

$$S_{11}=[(N_1^{/}\oplus N_{14}^{/})+N_{23}^{/}]+(P_{14} \oplus P_{23})$$

$$S_{13}=P_{14},\ S_{14}=N_{14}^{/} \quad (74)$$

$$S_{16}=P_1,\ S_{15}=N_1^{/} \quad (75)$$

Finally, in the case of m level design with CHBTMLI, the following expressions can be established through s number of H bridges or inputs. Although the switching and control technique is more complex in CHBTMLI, it reduces the component count in CHB design concerning all categories of input methods.

$$S_1=[(P_1 \oplus P_2) + (P_4 \oplus P_5)+\ldots\ldots\ldots+P_{(m-1)/2}] + [(N_2 \oplus N_3) + (N_5 \oplus N_6)+\ldots\ldots\ldots+(N_{(m-5)/2} \oplus N_{(m-3)/2})] \quad (76)$$

$$S_5=[(P_2 \oplus P_5) + (P_{11} \oplus P_{14})+\ldots\ldots\ldots+P_{(m-5)/2}] + [(N_5 \oplus N_8) + (N_{14} \oplus N_{17})+\ldots\ldots\ldots+ N_{(m-11)/2}]$$

$$S_9=[(P_5 \oplus P_{14}))+\ldots\ldots\ldots+P_{(m-17)/2}] + (N_{(m-53)/2} \oplus N_{(m-35)/2})$$

. . .
. . .
. . .

$$S_{4n-3}=P_{(m+3)/6}$$

$$S_2=[(N_1^{/}\oplus N_2^{/})+(N_4^{/}\oplus N_5^{/})+\ldots\ldots\ldots+N_{(m-1)/2}^{/}] + [(P_2 \oplus P_3) + (P_5 \oplus P_6)+\ldots\ldots\ldots+ (P_{(m-5)/2} \oplus P_{(m-3)/2})] \quad (77)$$

$$S_6=[(N_2^{/}\oplus N_5^{/})+(N_{11}^{/}\oplus N_{14}^{/})+\ldots\ldots\ldots+N_{(m-5)/2}^{/}] + [(P_5 \oplus P_8) + (P_{14} \oplus P_{17})+\ldots\ldots\ldots+ P_{(m-11)/2}]$$

$$S_{10}=[(N_5^{/}\oplus N_{14}^{/})+\ldots\ldots\ldots+N_{(m-17)/2}^{/}]+(P_{(m-53)/2} \oplus P_{(m-35)/2})$$

. . .
. . .
. . .

$$S_{4n-2} = N_{(m+3)/6}^{/}$$

$$S_3=[(N_1^{/}\oplus N_2^{/})+(N_3^{/}\oplus N_5^{/})+\ldots\ldots\ldots+N_{(m-3)/2}^{/}] + [(P_2 \oplus P_3) + (P_5 \oplus P_6)+\ldots\ldots\ldots+ (P_{(m-5)/2} \oplus P_{(m-3)/2})] \quad (78)$$

$$S_7=[(N_1^{/}\oplus N_5^{/})+(N_8^{/}\oplus N_{14}^{/})+\ldots\ldots\ldots+N_{(m-11)/2}^{/}] + [(P_5 \oplus P_8) + (P_{14} \oplus P_{17})+\ldots\ldots\ldots+ P_{(m-11)/2}]$$

$$
\begin{aligned}
&S_{11}=[(N_1^{/} \oplus N_{14}^{/})+\ldots\ldots\ldots+N_{(m-35)/2}^{/}]+(P_{(m-53)/2} \oplus P_{(m-35)/2})\\
&\quad . \qquad . \qquad .\\
&\quad . \qquad . \qquad .\\
&\quad . \qquad . \qquad .\\
&S_{4n-1}=N_1^{/}\\
&S_4=[(P_1 \oplus P_2)+(P_3 \oplus P_5)+\ldots\ldots\ldots+P_{(m-3)/2}]+[(N_2 \oplus N_3)+(N_5 \oplus N_6)+\ldots\ldots\ldots+(N_{(m-5)/2} \oplus N_{(m-3)/2})]\\
&S_8=[(P_1 \oplus P_5)+(P_8 \oplus P_{14})+\ldots\ldots\ldots+P_{(m-11)/2}]+[(N_5 \oplus N_8)+(N_{14} \oplus N_{17})+\ldots\ldots\ldots+N_{(m-11)/2}]\\
&S_{12}=[(P_1 \oplus P_{14})+\ldots\ldots\ldots+P_{(m-35)/2}]+(N_{(m-53)/2} \oplus N_{(m-35)/2})\\
&\quad . \qquad . \qquad .\\
&\quad . \qquad . \qquad .\\
&\quad . \qquad . \qquad .\\
&S_{4n}=P_1
\end{aligned}
\tag{79}
$$

V. SIMULATION RESULTS

The main objective of this work is to verify the logical expression as derived in the previous section through simulation and HIL for the different load conditions as well as for the grid-tied applications. For this reason, the proposed CHB inverters are simulated for both symmetrical and asymmetrical sources by using two and three H bridges. With two H Bridges, asymmetrical 7 & 9 levels are simulated for CHBBMLI and CHBTMLI. On the other hand, 13, 15, 19, and 27 levels have been simulated using 3 H bridges for CHBNSMLI, CHBBMLI, CHBQLMLI, and CHBTMLI, respectively. Each experiment has been tested for PD, POD, and APOD modulation and control techniques with the considerations listed in Table 10 for the different simulation parameters comprising proposed asymmetrical designs.

For CHBTMLI, eight switches are required for nine levels and 12 switches are necessary for 27 level design. Therefore 27 level design is the best output voltage realized with less number of switches. All the output voltages are generated for the same modulation index (MI), i.e., 1, the Switching frequency is 5 kHz for 7, 9 & 13 level design where it is kept 10 kHz for 15, 19 & 27 level design to get better THD spectrum as the frequency ratio changes the output THD values. The output THD value may be varied by changing the MI and frequency ratio of the MCPWM technique according to recommended applications.

Table 11 shows the THD value achieved for each MCPWM technique for the simulated levels to confirm the viability of the proposed control logics. It shows that the output voltage THD is achieved for each level design is less than 20% without filter, as specified by IEEE 519-2014. Besides, in the case of 27 level design, the output THD is much better and less than 5% that is 3.27% in APOD satisfactory for grid-connected or standalone PV applications. The THD values can also be varied by changing the modulation index of the system for each level design to merge with particular applications.

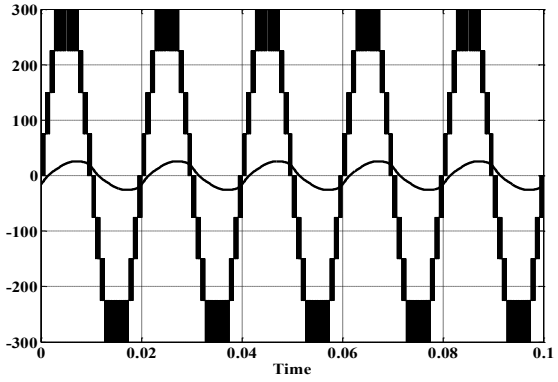
Table 10: Simulation parameter for all types of asymmetrical design

Design Parameters	**7 Level**	**9 Level**	**13 Level**	**15 Level**	**19 Level**	**27 Level**
Inverter Type	CHBBMLI	CHBTHMLI	CHBNSMLI	CHBBMLI	CHBQLMLI	CHBTHMLI
Switch Type	IGBT/Diode	IGBT/Diode	IGBT/Diode	IGBT/Diode	IGBT/Diode	IGBT/Diode
Modulating Signal	Sinusoidal (50Hz)	Sinusoidal (50Hz)	Sinusoidal (50Hz)	Sinusoidal (50Hz)	Sinusoidal (50Hz)	Sinusoidal (50Hz)
Carrier Signal	Triangular (5kHz)	Triangular (5kHz)	Triangular (5kHz)	Triangular (10kHz)	Triangular (10kHz)	Triangular (10kHz)
Input DC Voltages	V_1=100V V_2=200V	V_1=75V V_2=225V	V_1=50V V_2=100V V_3=150V	V_1=50V V_2=100V V_3=200V	V_1=35V V_2=70V V_3=210V	V_1=25V V_2=75V V_3=225V
Resistive Load	100Ω	100Ω	100Ω	100Ω	100Ω	100Ω

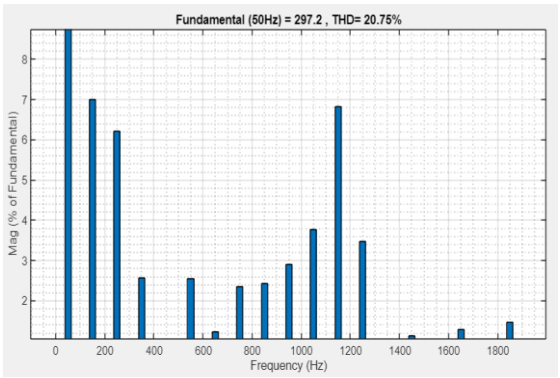
Proposed 9 and 27 level inverters, i.e., CHBTMLI, are considered and shown for RL load with 0.85 power factor as simulation output. Figure 3 and Figure 4 shows the output voltage and currents, including the current THD spectrum for 9 level and 27 level design with inductive load. The current THD is improved, and it is 8.46% for nine levels and 2.11% for 27 level design. This investigation further clarifies the correctness of the proposed inverters.

Table 11: Inverter level with corresponding THD value achieved at different MCPWM techniques

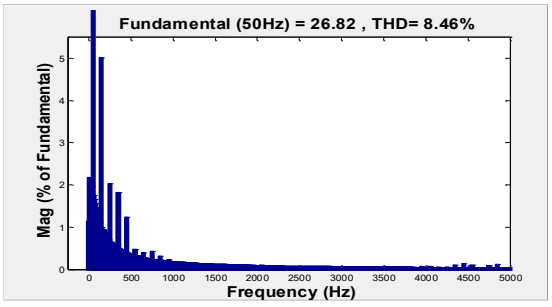
Level of inverter	THD value for different modulation techniques		
	PD	POD	APOD
7 level	17.32%	17.34%	16.88%
9 level	13.01%	12.07%	12.45%
13 level	9.36%	9.31%	9.35%
15 level	7.19%	7.13%	7.26%
19 level	5.64%	5.63%	5.65%
27 level	3.29%	3.28%	3.27%



(a)

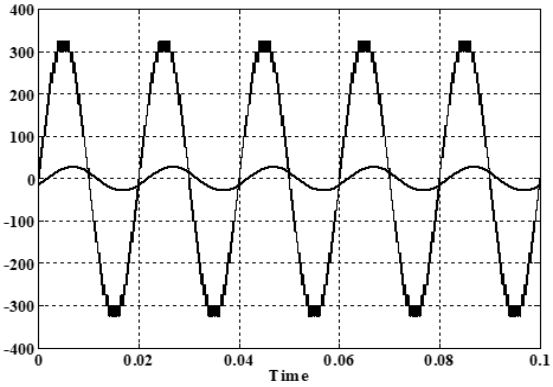


(b)

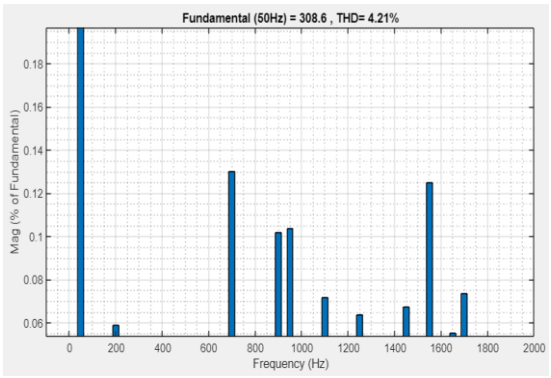


(c)

Figure 3: 9 level inverter design with RL load (a) output voltage and current (b) voltage FFT Spectrum (c) current THD spectrum



(a)



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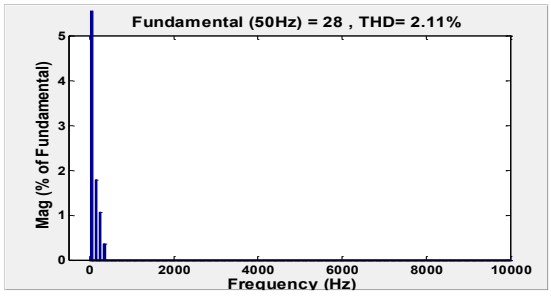


(c)

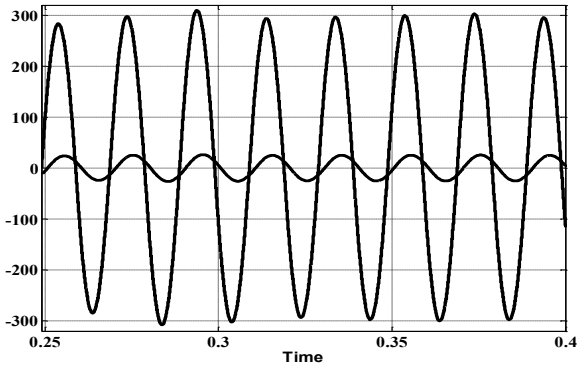
Figure 4: 27 level inverter design with RL load (a) output voltage and current (b) voltage FFT spectrum (c) current THD spectrum

VI. GRID TIED SYSTEM DESIGN

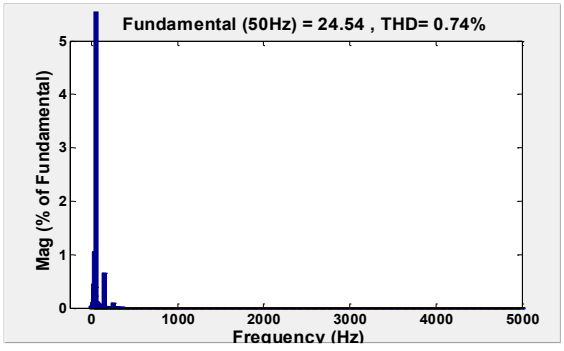
CHBTMLI is also simulated for grid integration considering the same input voltage pattern as simulation and the LCL filter is incorporated allowing 0.85 as a grid power factor. In this case, the filter parameter [30] is selected as $L_1=L_2=5mH$ and $C=4.4\mu F$ for both 9 and 27 level design, as depicted in Figure 5 and Figure 6. Here, the grid current THD value is much better than the value described by the different grid codes and standards. The grid current control system diagram for CHBTMLI 9 level inverter is shown in Figure 7. In this control diagram grid voltage is taken as reference to generate the angle θ (=ωt) through PLL block. The cos and sine function of the angle θ is obtained to get inverter reference current for the real and reactive power respectively. The inverter reference current is compared with the actual current and the error signal is allowed to pass through the PR controller [32] which is a modified version of PI controller. The PR controller is a mixture of a proportional term and a resonant term capable to eliminate the steady-state error completely as compared to PI controller. An additional feedback loop is added with PI controller to get the required and modified steady-state performance as shown in Figure 8. The transfer function of the PR controller is expressed below:-

$$T(s)=R(s)/E(s)=K_P+K_I\frac{s}{s^2+\omega^2} \tag{80}$$

The K_P and K_I value of the PR controller can be adjusted or changed for the required output and zero steady state performance for the particular design of the multilevel inverters. The ω value is always 100π. The K_P is estimated as 3.33 and the K_I value is taken as 100 [33]. The grid voltage is added with the output of the PR controller which is an error to produce the inverter reference voltage. The reference voltage is then compared with the carrier waves to develop MCPWM control and switch logic as given in expression 58 to 61, to create the inverter output voltage.

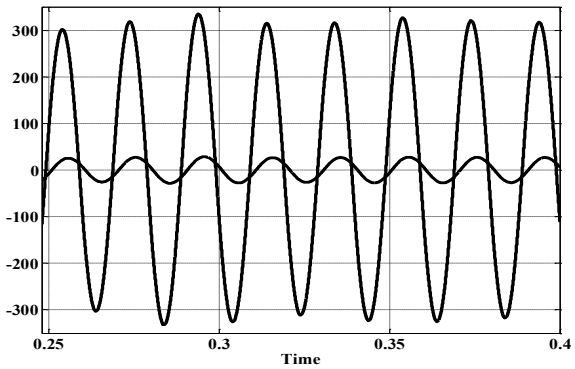


(a)

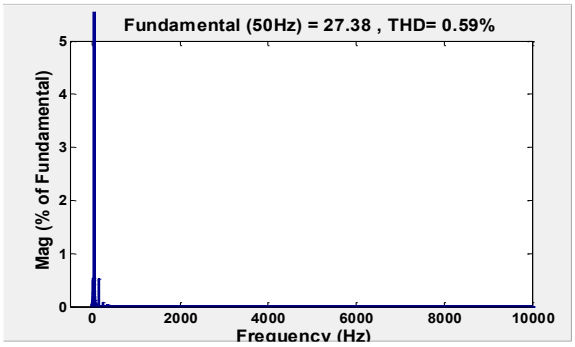


(b)

Figure 5: 9 level inverter with grid-tied application (a) grid voltage and current (b) grid current THD spectrum



(a)



(b)

Figure 6: 27 level inverter with grid-tied application (a) grid voltage and current (b) grid current THD spectrum

Grid current is controlled by changing the performance parameters of the system. When it is required to supply power to the grid from inverters the cosωt input is taken with required magnitude. For reactive power flow sinωt is taken from the PLL blocks. By this way, real and reactive power is injected to the grid. Besides, the modulation index of the MCPWM control can also be adjusted to achieve the required THD and power quality. Figure 9(a) shows the grid voltage, current, and inverter current are shown for real power injection. Also, the change of grid

current dynamism for the change of different system parameters is provided in Figure 9(b). It can be observed that inverter current increased from 5A to 10A by changing the reference of the inverter. The change of the reference current can be linked to the irradiation level and thus it will inject power to the grid according to the level of irradiation.

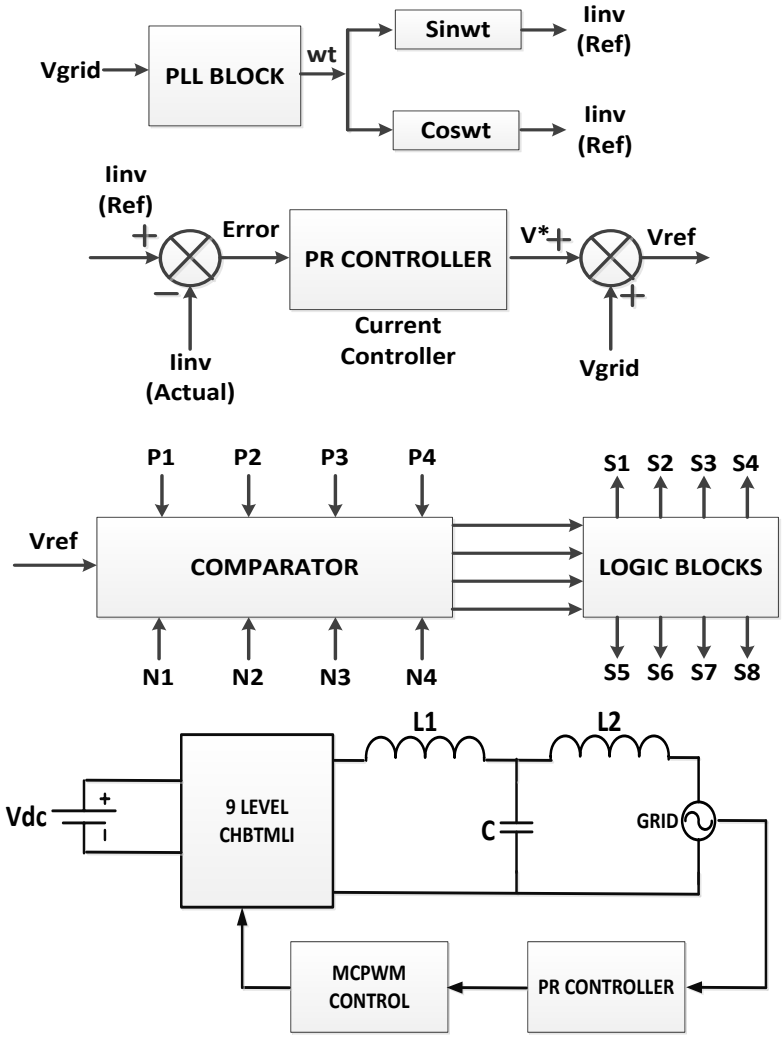


Figure 7: Grid-current control system diagram for 9 level design

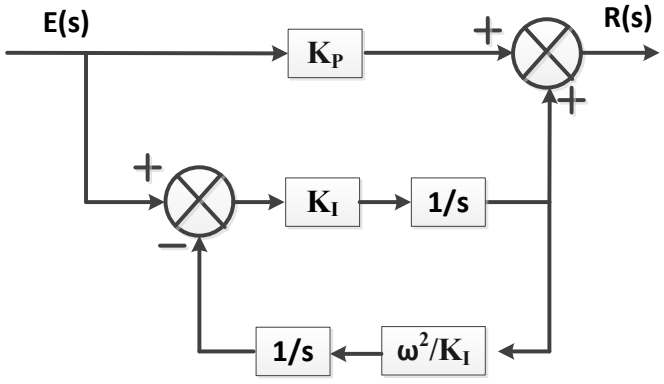


Figure 8: PR controller block

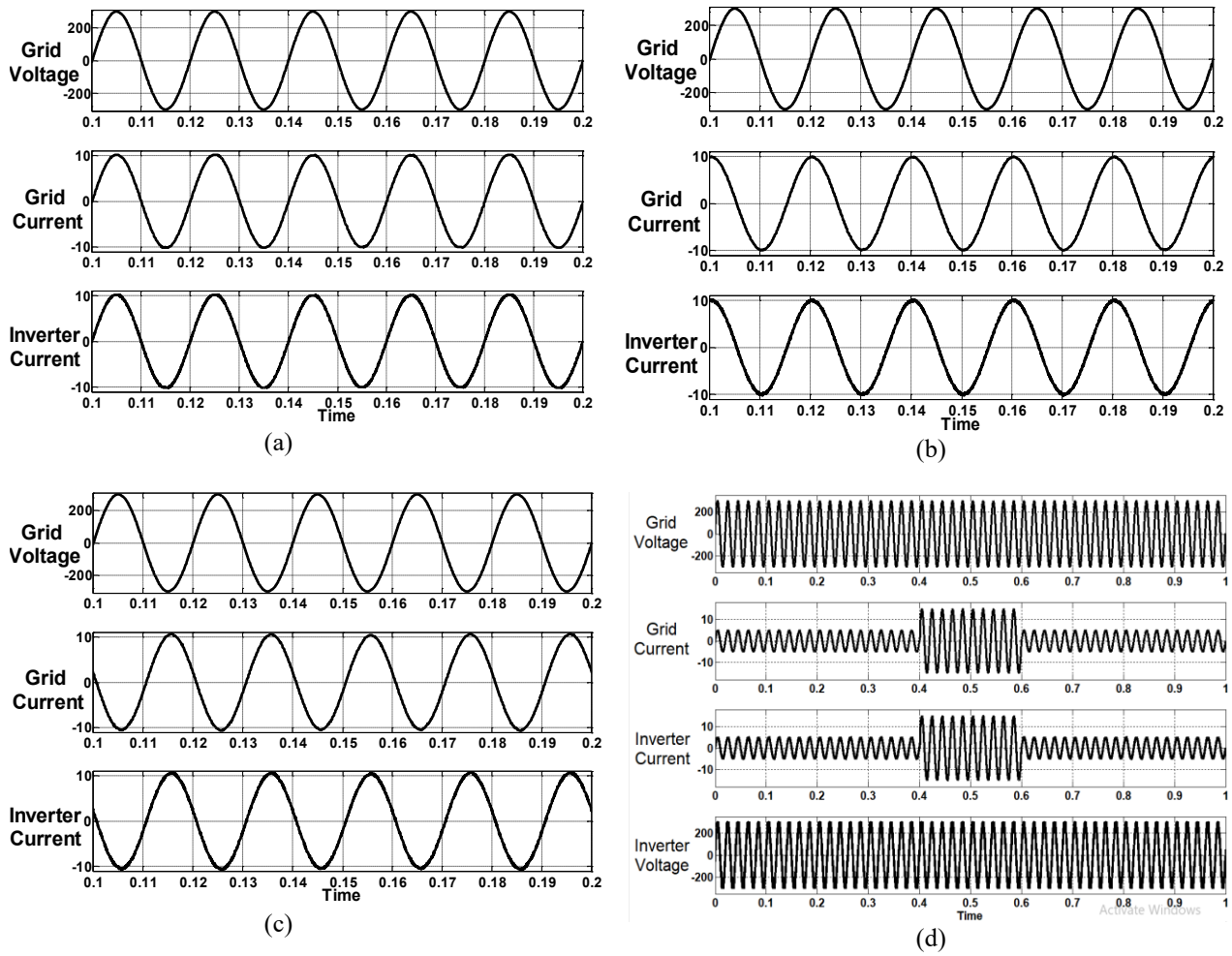


Figure 9: (a) Grid voltage and current for real power injection, (b) when grid current leads the grid voltage, (c) when grid current is 180 degree opposite to grid voltage, (d) dynamic behaviour of the grid current for changing the system parameters

VII. DISSCUSSION & FINDINGS

Table 12 shows the mathematical formulation of switches and component counts for all proposed inverters with m level for single-phase applications. For three-phase inverter design, the component count must be multiplied by three and the line to line voltage will be (2m-1) for m level phase voltage where third harmonics will be rejected automatically. For example, if the phase to neutral voltage is 9 level in single-phase design, the line to line voltage will be 17 level in three-phase inverter design, which also improves the output THD value significantly. Figure 10 displays the reduction in the component count for asymmetrically switched CHB inverter design.

If 81 level inverter is needed to be designed, then it requires 16 switches with 16 primary diodes, four dc sources, and the total component count will be 36 according to different mathematical expressions shown in Table 12. From Figure 10, it is realized that CHBTMLI has less switch and component count with respect to other proposed CHB inverters. Therefore, it discloses that CHB inverters can be utilized for reduced switch topology with significantly reduced component counts to achieve high output levels, including high power quality.

Table 12: Mathematical formulation of Component counts for m level design of all the proposed CHB inverters

Component type	CHBMLI	CHBNSMLI	CHBBMLI	CHBQLMLI	CHBTMLI
Number of main switches	2(m-1)	2×{√(4m-3)-1}	4/log2[log{(m+1)/2}]	2×√(4m+93)-14	(4/log3)logm
Number of main diodes	2(m-1)	2×{√(4m-3)-1}	4/log2[log{(m+1)/2}]	2×√(4m+93)-14	(4/log3)logm
Number of DC sources	(m-1)/2	{√(4m-3)-1}/2	[log{(m+1)/2}]/log2	{2×√(4m+93)-14}/4	logm/log3
Total count	9×(m-1)/2	9×{√(4m-3)-1}/2	9×[log{(m+1)/2}]/log2	9×{2×√(4m+93)-14}/4	9×logm/log3

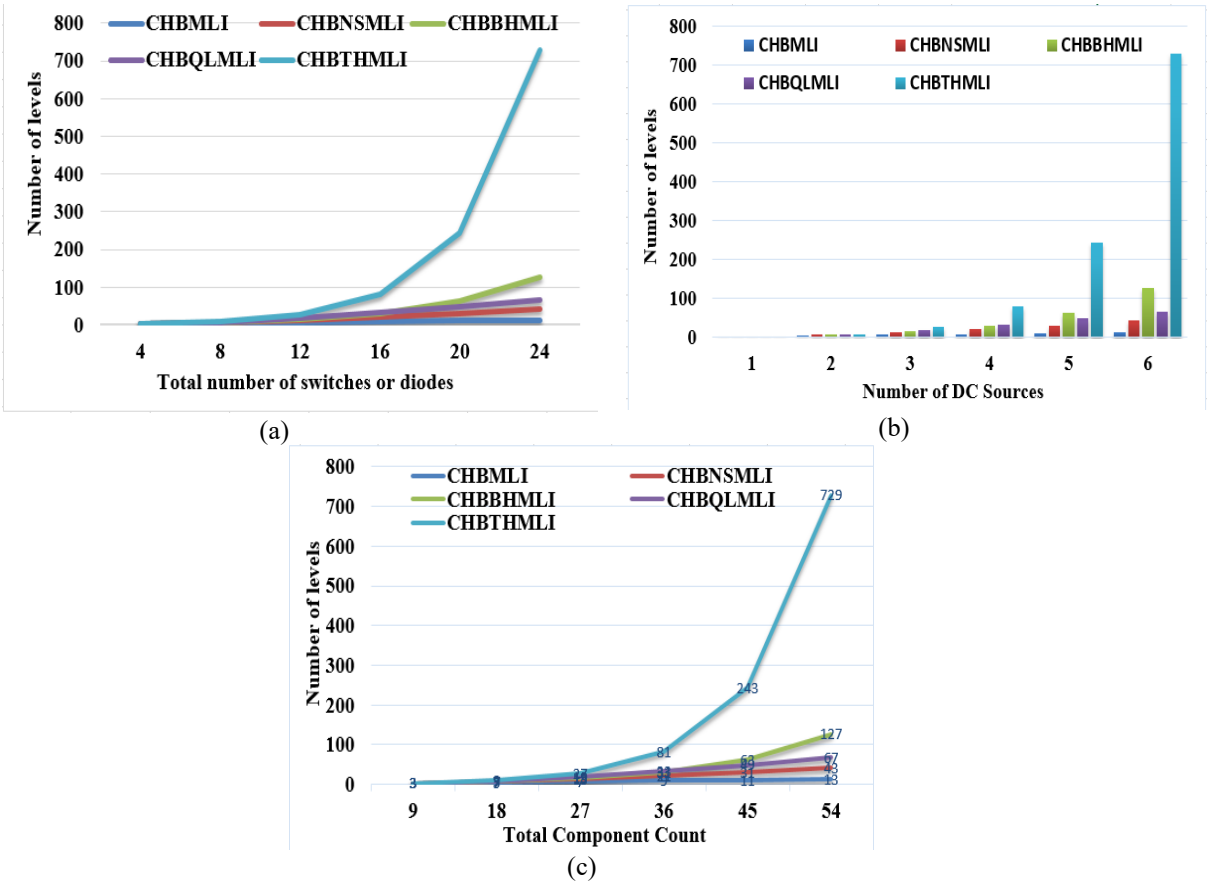


Figure 10: Comparison of CHB inverters according to designed levels with respect to (a) total number of switches or diodes (b) number of dc sources (c) total component count

VIII. HIL VERIFICATION

Asymmetrically switched, all the proposed inverters are verified and tested through OPAL-RT (OP5600) testbed in a hardware-in-the-loop (HIL) environment. HIL testing is a technique where real-time signals from a controller are associated with a test system that simulates reality, designating the controller into thinking it is in the assembled product. So, real-time simulations are necessary to project and verify the system's capability, performance, and exactness. Models that are already developed through MATLAB simulations can be established in a real-time environment as like as actual physical system.

The OPAL-RT is the PC/FPGA-based real-time simulators that include HIL testing equipment and Rapid Control Prototyping (RCP) systems to design, test, and optimize control and protection systems used in different industrial applications. The OP5600 is a high-performance module that interacts with the MATLAB/Simulink environment of SimPowerSystem through a dedicated software called RT-Lab. OP5600 is suitable for very high-frequency switching and control of the power converters which is not generally facilitated by the other controllers [34].

To implement all the proposed asymmetrical inverter in real-time mode, first of all, the MATLAB simulations are edited and debugged at RT- Lab software of OPAL-RT. After that, the programs are built-in that real-time environment. When programs are built successfully, they are loaded in the OPAL-RT module for HIL synchronization. Finally, all the programs are executed, and the corresponding real time data are taken through DSO and power analyzer. The real time experimental setup is shown in Figure 11.

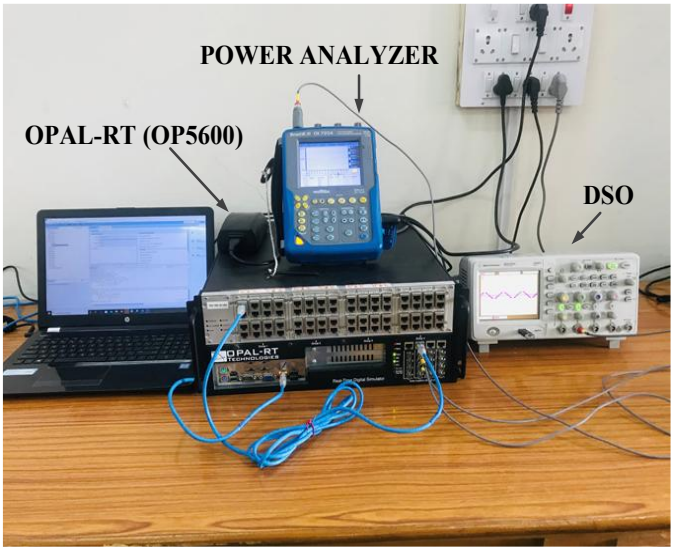
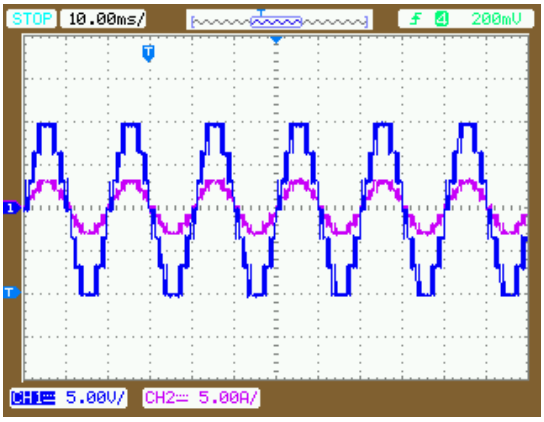
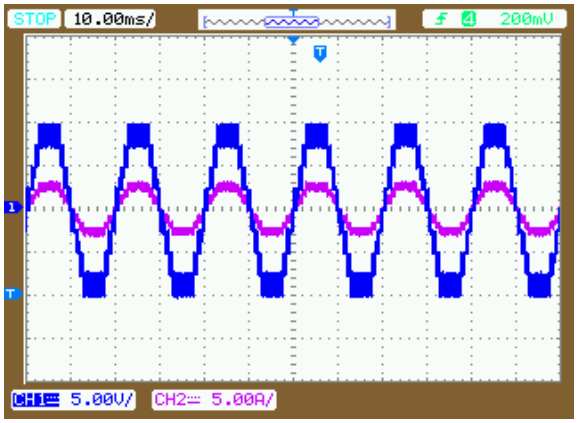


Figure 11: HIL testbed with OPAL-RT (OP5600) module.

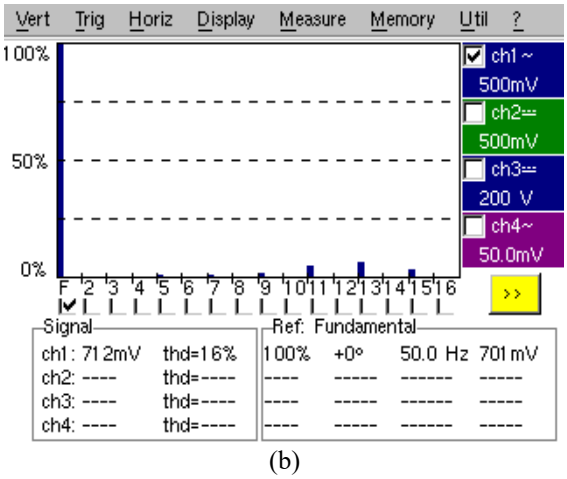
Figure 12 to 17 shows the output voltage and currents with the voltage THD spectrum for all the proposed levels, i.e., 7, 9, 13, 15, 19 & 27, respectively. All the real-time results are reduced within the range of ±16V/A as OPAL-RT output supports on that range. Figure 18 shows the real time implementation of the grid-tied 9 level inverter which incorporates grid voltage, grid current and the inverter current for the control system designed during the simulation. For the operation of the reactive power flow, the 90 degrees and 180 degrees phase shifted results are shown in Figure 18 (b) & (c). HIL results realized the feasibility of proposed MCPWM based switching techniques of the suggested multilevel inverters.



(a)



(a)



(b)

Figure 12: Asymmetrical 7 level inverter (a) output voltage and current (b) voltage THD spectrum

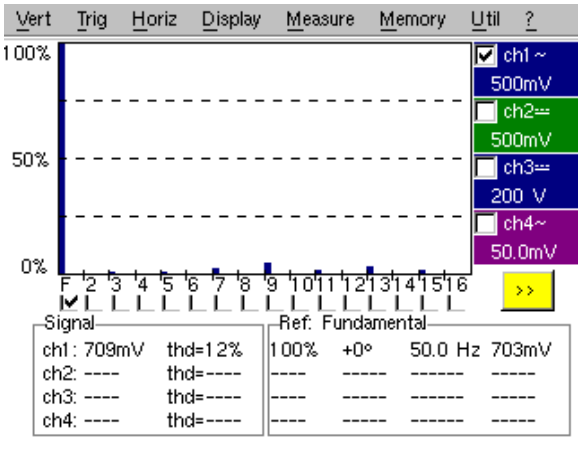
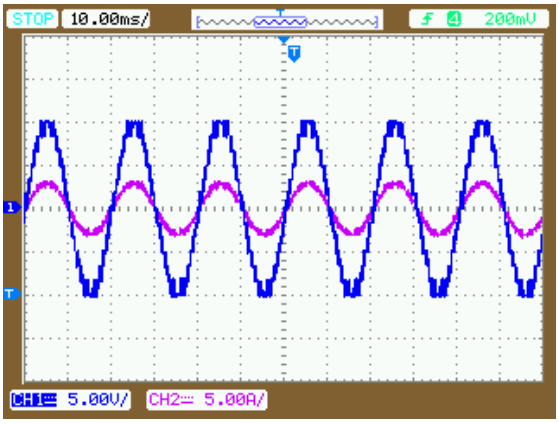
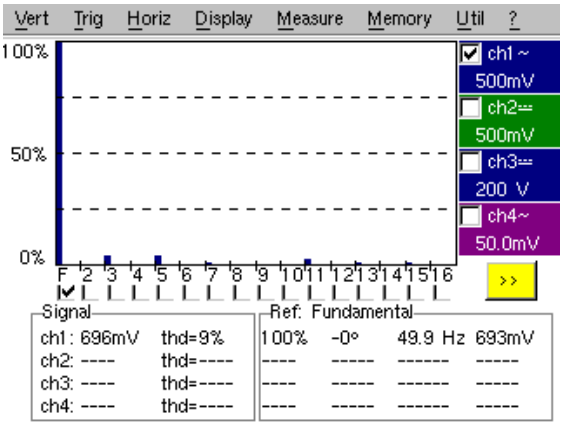


Figure 13: Asymmetrical 9 level inverter (a) output voltage and current (b) voltage THD spectrum

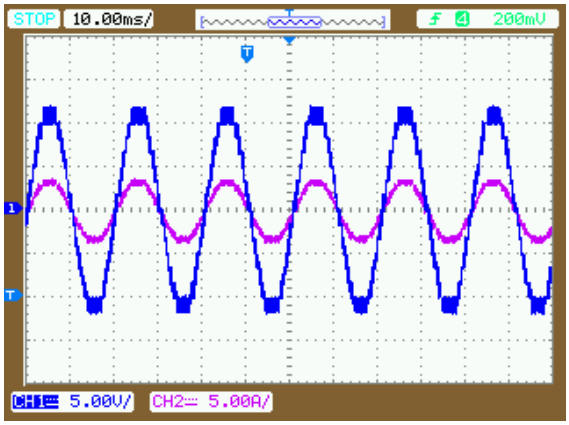


(a)

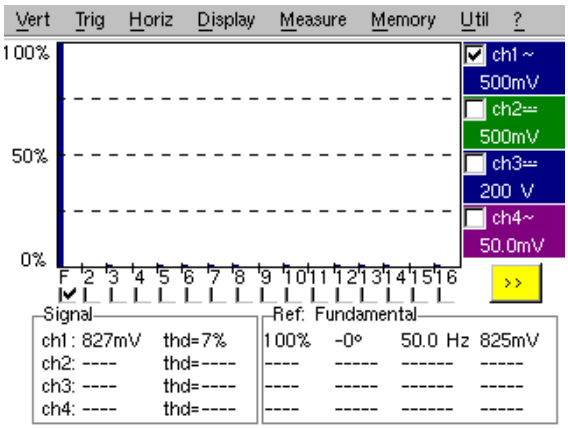


(b)

Figure 14: Asymmetrical 13 level inverter (a) output voltage and current (b) voltage THD spectrum

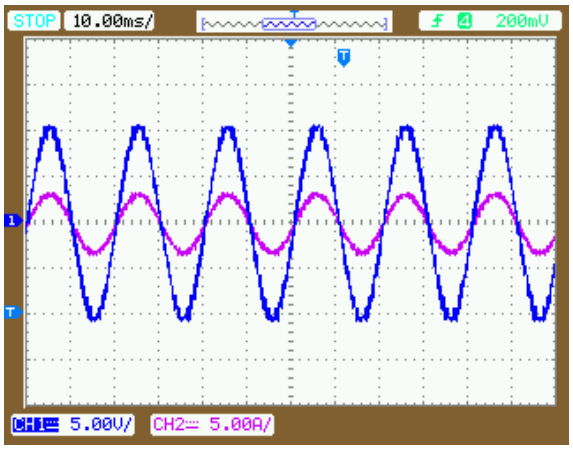


(a)

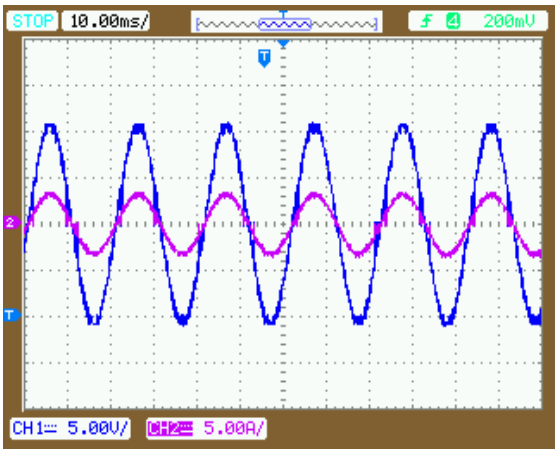


(b)

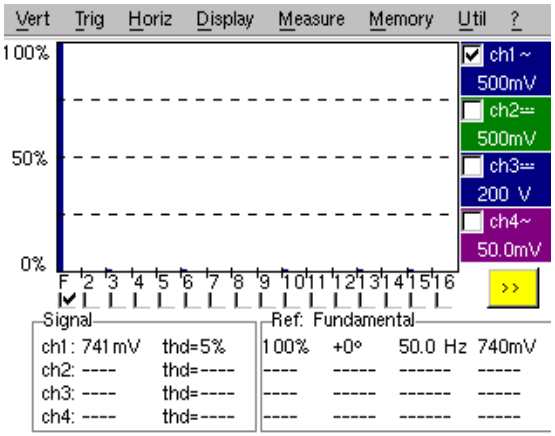
Figure 15: Asymmetrical 15 level inverter (a) output voltage and current (b) voltage THD spectrum



(a)

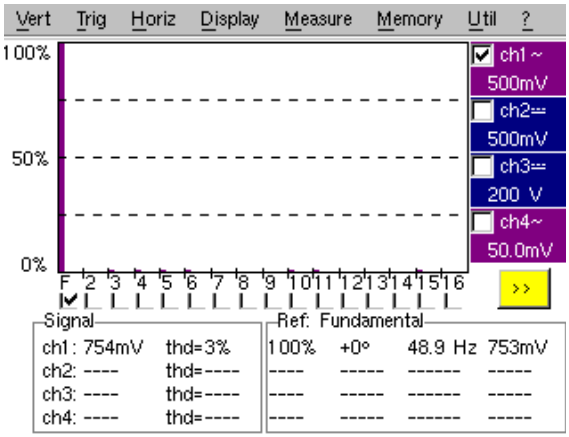


(a)



(b)

Figure 16: Asymmetrical 19 level inverter (a) output voltage and current (b) voltage THD spectrum



(b)

Figure 17: Asymmetrical 27 level inverter (a) output voltage and current (b) voltage THD spectrum

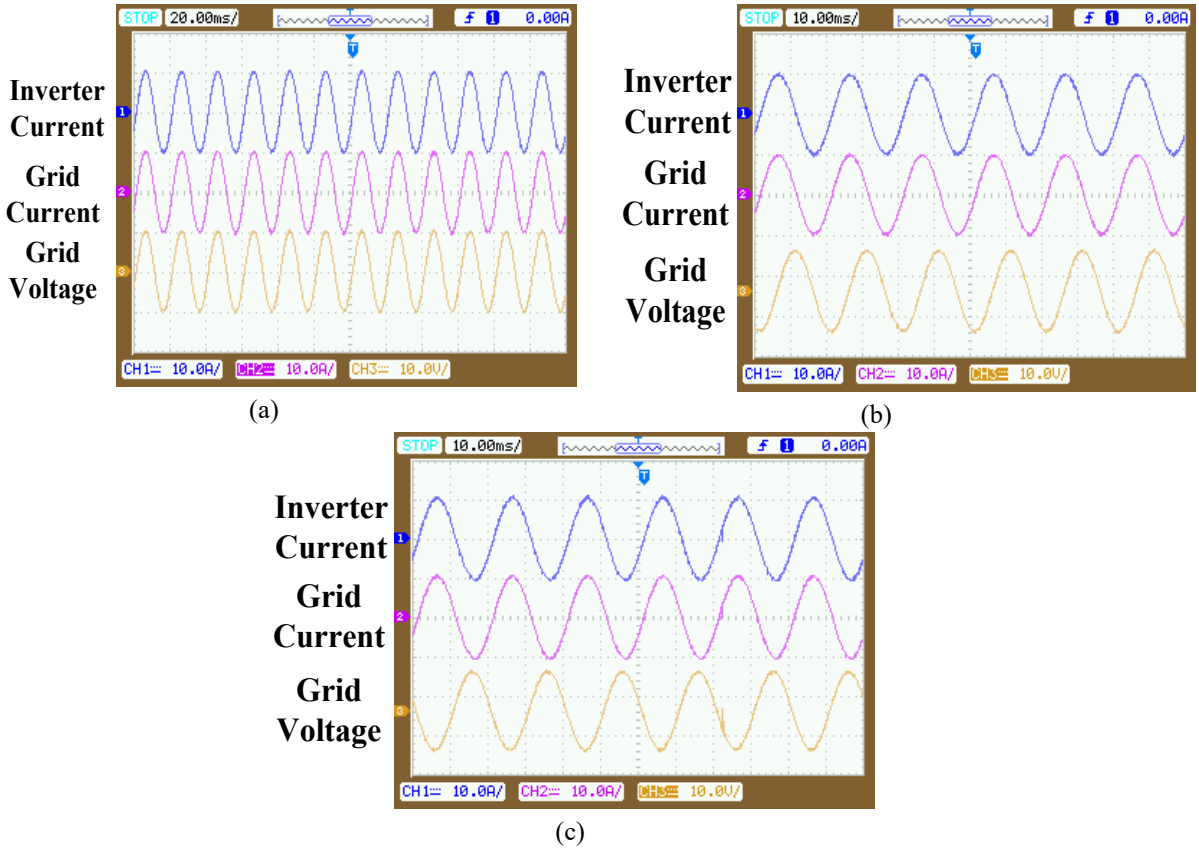


Figure 18: Grid voltage, grid current and inverter current for the grid-tied 9 level inverter (a) with unity power factor (b) grid current 90 degrees phase shifted (c) grid current 180 degrees phase shifted

IX. Inverter Performance for Standalone Applications

To verify the inverter performance with different irradiation and constant temperature a two input CHBTMLI is considered. It is already known that for the asymmetrical two input CHBTMLI nine level can be generated. In the simulation study the irradiance level is changed from 100W/m^2 to 1000w/m^2 maintaining a constant temperature 25^{0}C. To maintain the asymmetrical input voltage the PV array is adjusted with MPPT control to generate the nine level output. The block diagram of the simulated model is given in Figure 19. Conventional perturb and observe based MPPT control is utilized here to get the maximum power through boost converter. Figure 20 (a) shows the nine level output voltage and current with constant irradiance of 1000W/m2 and Figure

20(b) shows the variation in the output voltage and current with different irradiation. Hence, Figure 20 proves the efficacy of the proposed topology for asymmetrical two inputs 9 level (CHBTMLI) with constant and variable irradiation.

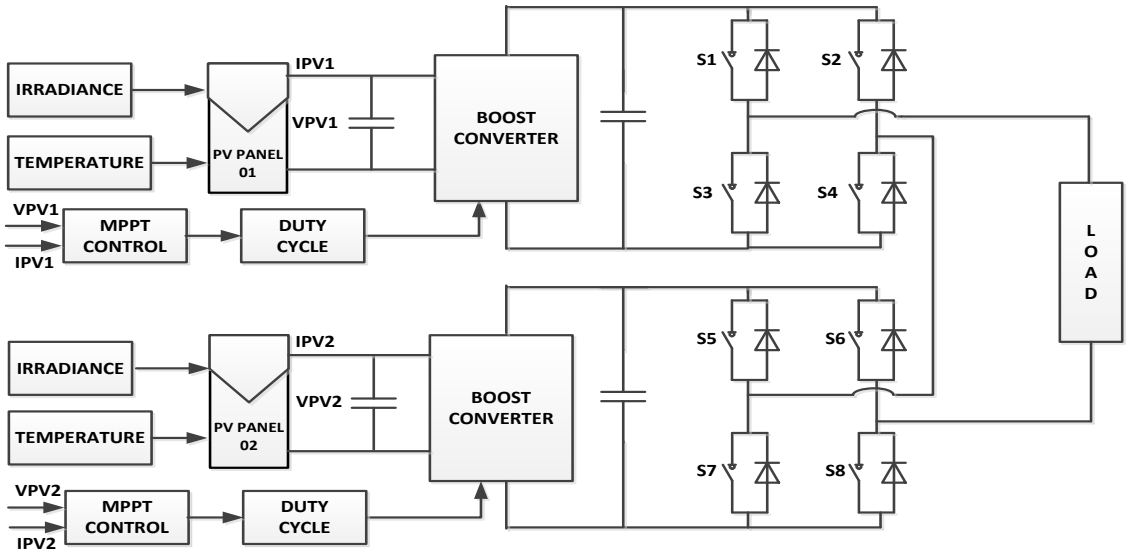
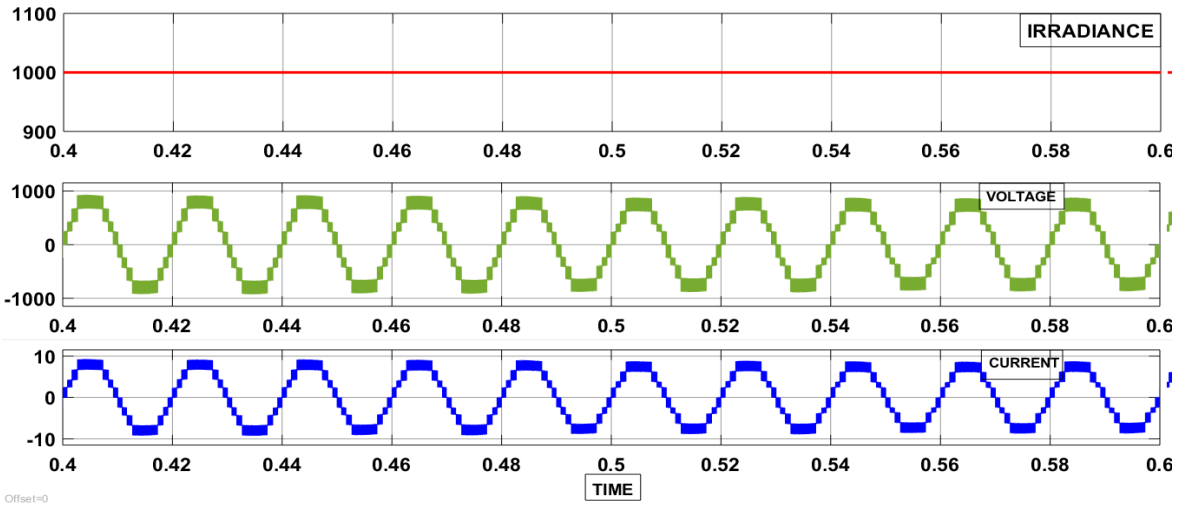
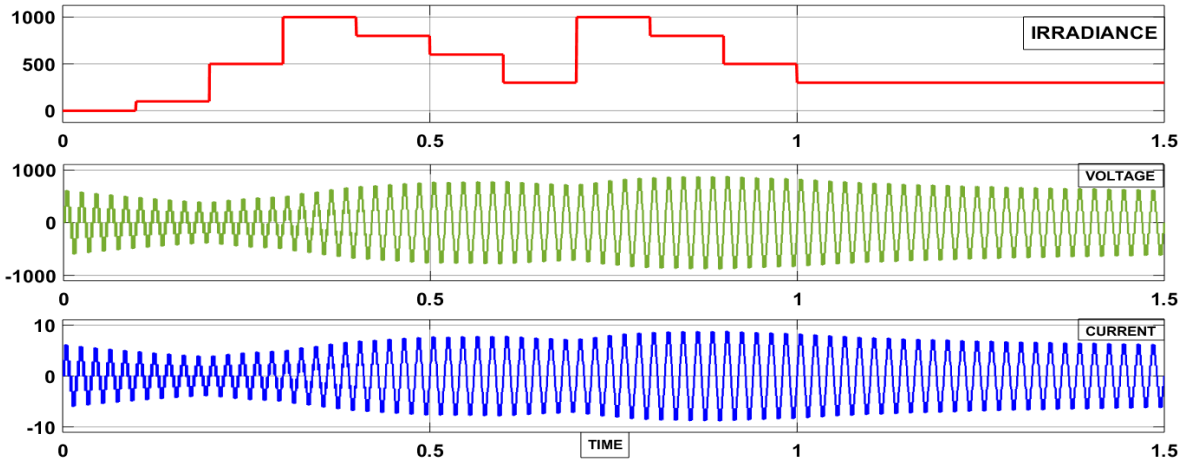


Figure 19: Block diagram of the simulated model for the different irradiation with the proposed 9 level inverter



(a)



(b)

Figure 20: Output voltage and current (a) for constant irradiance (b) for irradiance variation

The proposed research work essentially realizes the potentiality of CHB inverters to generate with any number of output voltage levels as there is a provision for additive and subtractive voltage switching at CHB topology. The major limitation of the proposed techniques as with the increase of number of levels pressure on each switch is not identical because of asymmetrical inputs and this can be addressed by using modified control strategies at the input side for stand-alone or grid-tied applications.

X. CONCLUSION

To implement switch control logic perfectly, different Boolean expressions are considered to develop elaborated and simplified switch logic for the proposed MCPWM based control techniques. The modular expressions in MCPWM techniques are suitable for equal and unequal voltage switching at CHB inverter design, with required output voltages is verified through the MATLAB/Simulink environment. The THD value for different MCPWM techniques is shown, and improved THD, i.e., power quality is achieved because of high-level design with asymmetrical switching. CHBTMLI is considered and simulated for inductive load and grid-tied power generation with LCL filter. The simulation and HIL results are incorporated to prove the practicality of the proposed all types of structures. All the simulation results have been tested using real-time HIL implementation, which reveals the viability of the proposed inverters. The component count of the proposed topologies is reduced when it is designed at CHBTMLI. CHBTMLI is the best possible design with high power quality and efficiency, as well as the lowest switch count, according to IEEE 519-2014. The authors' contribution mainly focused on the developing of the control logic and expressions including the scaled version of all possible types of CHB inverters, either symmetrical or asymmetrical switching. The grid-tied application of the CHBTMLI with 9 level also discloses the viability of the proposed asymmetrical switching. The proposed inverters are suitable for renewable power generation, especially for solar PV applications as it can be integrated separately according to topological advantages.

REFERENCES

[1] K. Wang, Z. Zheng, L. Xu and Y. Li, "Neutral-Point Voltage Balancing Method for Five-Level NPC Inverters Based on Carrier-Overlapped PWM," in IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1428-1440, Feb. 2021

[2] R. H. Baker. Switching Circuit. U. S. Patent 4210826, 1980.

[3] C. B. Barth et al., "Design and Control of a GaN-Based, 13-Level, Flying Capacitor Multilevel Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 3, pp. 2179-2191, Sept. 2020.

[4] J. P. Lavieville, P. Carrere, T. Meynard, Electronic Circuit for Converting Electrical Energy and a Power Supply Installation Making Use Thereof. U. S. Patent 5668711 (1997).

[5] R. Sarker, A. Datta and S. Debnath, "An Improved Multicarrier PWM (MCPWM) Technique With a New Harmonic Mitigation Strategy for Cascaded H-Bridge Multilevel Inverter Applications," in IEEE Transactions on Industrial Informatics, vol. 18, no. 3, pp. 1500-1510, March 2022.

[6] Nithin Raj, Anjali Anand, G. Jagadanand and Saly George, "Development and experimental validation of fault detection and diagnosis method in SPWM modulated symmetric cascaded H-bridge multilevel inverter," in *International Journal of Power Electronics*, Vol. 11, No. 3, pp. 409-426, 2020.

[7] Elena Villanueva, Pablo Correa, José Rodríguez, and Mario Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Transactions on Industrial Electronics*, Vol. 56, no. 11, pp. 4399 – 4406, Nov. 2009.

[8] Bhupender Sharma, Ratna Dahiya, Jayaram Nakka, "Effective grid connected power injection scheme using multilevel inverter based hybrid wind solar energy conversion system," *Electric Power Systems Research*, Vol. 171, pp. 1-14, June 2019.

[9] J. Venkataramanaiaha, Y. Suresha, Anup Kumar Pandab, "A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies," *Renewable and Sustainable Energy Reviews*, Vol. 76, pp. 788-812, Sept. 2017.

[10] Faouzi Armi, Lazhar Manai and Mongi Besbes, " Cascaded H-bridge inverter with reduced device count control considering harmonic distortion minimisation," in International Journal of Power Electronics, Vol. 11, No. 2, pp 139–159, 2020.

[11] Jagabar Sathik Mohd.Ali, Vijayakumar Krishnaswamy, "An assessment of recent multilevel inverter topologies with reduced power electronics components for renewable applications," *Renewable and Sustainable Energy Reviews*, Vol. 82, pp. 3379-99, Feb. 2018.

[12] Mariusz Malinowski, K. Gopakumar, Jose Rodriguez, and Marcelo A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, Vol. 57, no. 7, pp. 2197-2206, July 2010.

[13] Fang Lin Luo & Hong Ye. *Advanced dc/ac inverters: applications in renewable energy*, 1st ed. Tailor and Francis Group: CRC Press, 2013.

[14] Nor Shahida Hasan, Norzanah Rosmin, Dygku. Asmanissa Awg. Osman, Aede Hatib Musta'amal@Jamal, "Reviews on multilevel converter and modulation techniques," *Renewable and Sustainable Energy Reviews*, Vol. 80, pp. 163-74, Dec. 2017.

[15] Shubhajit Pal, Rubell Sen Goopta, Muneer V, Avik Bhattacharya, "Power Quality Improvement of a Reduced Switch MLI Using a Modified ANN-Based SHE Technique," in IETE Technical Review, Vol. 40, No. 4, pp. 591-607, 2023.

[16] Rubell Sen Goopta & Avik Bhattacharya, “Reduced switch multilevel inverter with symmetrical & asymmetrical dc sources for solar PV applications,” in *Proceedings of the IEEE Region 10 Symposium (TENSYMP)*, Dhaka, Bangladesh, 2020, pp. 1468-73.
[17] M. H. Nguyen and S. Kwak, "Predictive Nearest-Level Control Algorithm for Modular Multilevel Converters With Reduced Harmonic Distortion," in IEEE Access, vol. 9, pp. 4769-4783, 2021.
[18] Perez M, Rodriguez J, Pontt J, Kouro S, “Power distribution in hybrid multi-cell converter with nearest level modulation,” in *Proceedings of the IEEE International Symposium on Industrial Electronics*, Vigo, Spain, 2007, pp. 736-41.
[19] Mohamed S. A. Dahidah, Georgios Konstantinou and Vassilios G. Agelidis, “A review of multilevel selective harmonic elimination PWM: formulations, solving algorithms, implementation and applications,” *IEEE Transactions on Power Electronics*, Vol. 30, no. 8, pp. 4091 – 4106, August 2015.
[20] A. Lewicki, I. C. Odeh and M. Morawiec, "Space Vector Pulsewidth Modulation Strategy for Multilevel Cascaded H-Bridge Inverter With DC-Link Voltage Balancing Ability," in IEEE Transactions on Industrial Electronics, vol. 70, no. 2, pp. 1161-1170, Feb. 2023.
[21] Natarajan Prabaharan, Kaliannan Palanisamy, “A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications,” *Renewable and Sustainable Energy Reviews*, Vol. 76, pp. 1248-82, Sept. 2017.
[22] S. K. Sahoo and T. Bhattacharya, "Phase-Shifted Carrier-Based Synchronized Sinusoidal PWM Techniques for a Cascaded H-Bridge Multilevel Inverter," in IEEE Transactions on Power Electronics, vol. 33, no. 1, pp. 513-524, Jan. 2018.
[23] Brendan Peter McGrath and Donald Grahame Holmes, “Multicarrier PWM strategies for multilevel inverters,” *IEEE Transactions on Industrial Electronics*, Vol. 49, no. 4, pp. 858-67, 2020; 49 (4): 858-67.
[24] K. K. Gupta & Pallavee Bhatnagar. *Multilevel inverters conventional and emerging topologies and their control*, 1st ed. Cambridge, MA, Academic Press: Elsevier, 2018.
[25] M. Morris Mano. *Digital logic and computer design*, 1st ed. India: Pearson, 2016.
[26] Ronald J Tocci, Neal S. Widmer, Gregory L. Moss. *Digital systems: principles and applications*, 10th ed. India: Pearson, 2009.
[27] IEEE standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces. *IEEE Std 1547-2018*, 2018.
[28] N. Rigogiannis, N. Delianidis, I. Mandourarakis, N. Papanikolaou and E. Koutroulis, "Feasibility Study of a Fully Decentralized Control Scheme for PV Cell-Level Cascaded H-Bridge Inverters," in IEEE Access, vol. 11, pp. 69826-69840, 2023.
[29] IEEE recommended practice and requirements for harmonic control in electric power systems. *IEEE 519-2014*, 2014.
[30] Aleksandr Reznik, Marcelo Godoy Simões, Ahmed Al-Durra, and S. M. Muyeen, “LCL filter design and performance analysis for grid-interconnected systems,” *IEEE Transactions on Industry Applications*, Vol. 50, no.2, pp. 1225-32, March-April 2014.
[31] Bao Xie, Ke Guo, Mingxuan Mao, Lin Zhou, Tiantian Liu, Qianjin Zhang, and Gaofeng Hao, “Analysis and improved design of phase compensated proportional resonant controllers for Grid-Connected inverters in Weak Grid,” *IEEE Transactions on Energy Conversion*, Vol. 35, no. 3, pp. 1453-64, Sept. 2020.
[32] Rachid Errouissi, Hussain Shareef, Addy Wahyudie, “A Novel Design of PR Controller with Anti-windup Scheme for Single-Phase Interconnected PV Systems,” *IEEE Transactions on Industry Applications*, Vol. 57, no. 5, pp. 5461-75, Sept./Oct. 2021.
[33] Bao Xie, Ke Guo, Mingxuan Mao, Lin Zhou, Tiantian Liu, Qianjin Zhang, Gaofeng Hao, “Analysis and Improved Design of Phase Compensated Proportional Resonant Controllers for Grid-Connected Inverters in Weak Grid,” *IEEE Transactions on Energy Conversion*, Vol. 35, no. 3, pp. 1453-64, Sept. 2020
[34] OPAL-RT Technologies. *https://www.opal-rt.com/*, 2022 [accessed 31 May, 2025].